

GLAST Large Area Telescope Calorimeter Subsystem

8.0 EEE Parts and Electronic Packaging

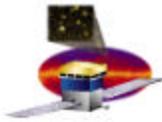
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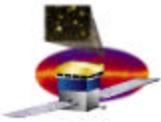




Outline

- **EEE Parts Requirements**
- **EEE Part Implementation Plan**
- **EEE Parts Status**
- **Plastic Encapsulated Microcircuits (PEMs)**
- **Process Flow Chart for ASICs**
- **Process Flow Chart for PEM screening**
- **EEE Parts Concerns**
- **Radiation Testing**
- **Radiation testing Results**
- **Electronic Packaging Program**
- **Manufacturing and Test Process Flow of CAL Hardware**

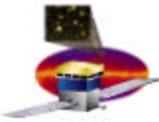




EEE Parts Requirements

- **Requirements Summary**
 - **Parts screening and qualification per GSFC 311-INST-001, Level 2**
 - **Additional requirements outlined in the LAT EEE parts program control plan, LAT-MD-00099-1**
 - **Review and approve EEE Part Lists**
 - **Derate EEE Parts per PPL-21**
 - **Review and approve derating information before drawing sign-offs**
 - **Perform stress analysis**
 - **Parts Control Board (PCB) Approach, a partnership arrangement with NASA/GSFC parts engineer and code 562**

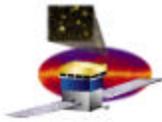




EEE Parts Implementation Plan

- Part lists are reviewed and approved by the project PCB prior to flight procurements
- Special considerations include:
 - Radiation evaluation of all active components
 - Radiation testing (TID and/or SEE) when necessary
 - Parts stress analysis
 - PIND testing on all cavity devices
 - Destructive Physical Analysis (DPA), when applicable
 - Pre Cap or sample DPA on semiconductors, microcircuits and hybrids devices as required
 - Life Testing if Quality Conformance Inspection (QCI) data within one year of the lot being procured is not available
 - No pure tin, cadmium, and zinc plating is allowed

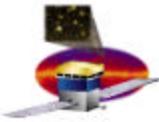




EEE Parts Implementation Plan

- **Special considerations include cont'd:**
 - **50V ceramic capacitors require 85°C/85RH low voltage testing**
 - **Mandatory surge current testing on all tantalum capacitors**
 - **Plastic Encapsulated Microcircuits requires special evaluation as outline in the EEE parts plan**
 - **Age control requirements. Lot Date Code (LDC) older than 9101 requires DPA and room temperature re-screen**
 - **Parts traceability from procurement to assembly of boards**
 - **GIDEP Alerts & NASA Advisories review and disposition**
 - **Parts Identification list (PIL) includes LDC, MFR, Radiation information on the flight lot**

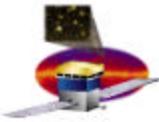




EEE Parts Status

- The CAL subsystem EEE parts lists have been reviewed by the PCB and all parts have been approved except PEM parts and connectors
- Discuss EEE parts availability weekly, to support fabrication schedule which includes:
 - Call manufacturers and suppliers to expedite delivery as required
 - Work with test facilities to expedite delivery schedule
- Perform 100% incoming inspection
- Performed stress analysis of all parts on the parts lists and met derating criteria after stress application
- Perform screening and qualification tests as required
- Held regular meeting with GSFC Parts Engineer to resolve any parts-related issues and approve parts through the Parts Control Board (PCB)
- Attribute data for screening and lot specific qualification/QCI data shall be reviewed for acceptance of parts for flight
- Parts Identification List (PIL) and As-built parts lists is maintained

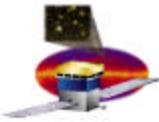




Plastic Encapsulated Microcircuits (PEMs) (Packaged parts, ASICs, ADC, DAC)

- **Total 4 types of PEMs used on CAL AFEE board**
- **ASICs are fabricated using Agilent processes and packaged by ASAT Hong Kong (QML approved)**
- **ADC and DAC are manufactured by Maxim from a single wafer and assembly lot and parts are fully tested prior to receipt at NRL**
- **PEM parts will be sample screened (min. 10% of lot size, lot size to be greater than 200 pieces) which includes temperature cycle, initial electrical parameters, dynamic burn-in, final electrical tests which includes static test at +25 degrees C, dynamic and functional at +25 degrees C, and switching test at +25 degrees C, CSAM, and final visual**
- **Screening data shall be reviewed for use of balance quantity on the lot for flight applications**

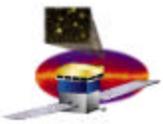




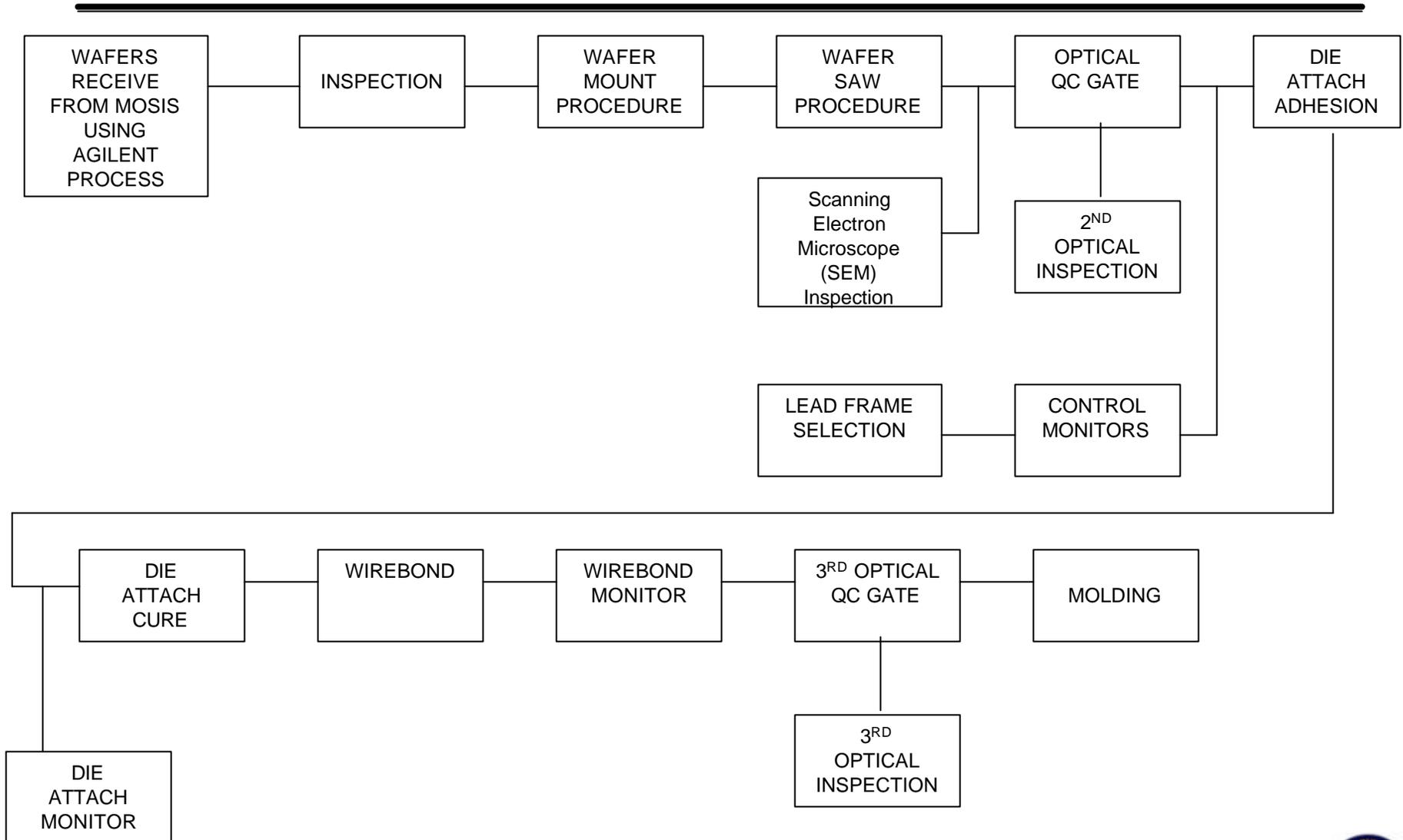
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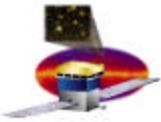
- **Each screened PEM type will be qual tested which includes DPA, preconditioning, temperature cycling, HAST, CSAM, and electrical test**
- **Assembled PWB will be subjected to environmental stress screening (ESS) prior to conformal coating, which includes thermal cycling, dynamic burn-in at -30 degrees C to $+85$ degrees C, and 100% visual inspection**
- **All parts will be handled using ESD precautions and will be stored in nitrogen cabinets**



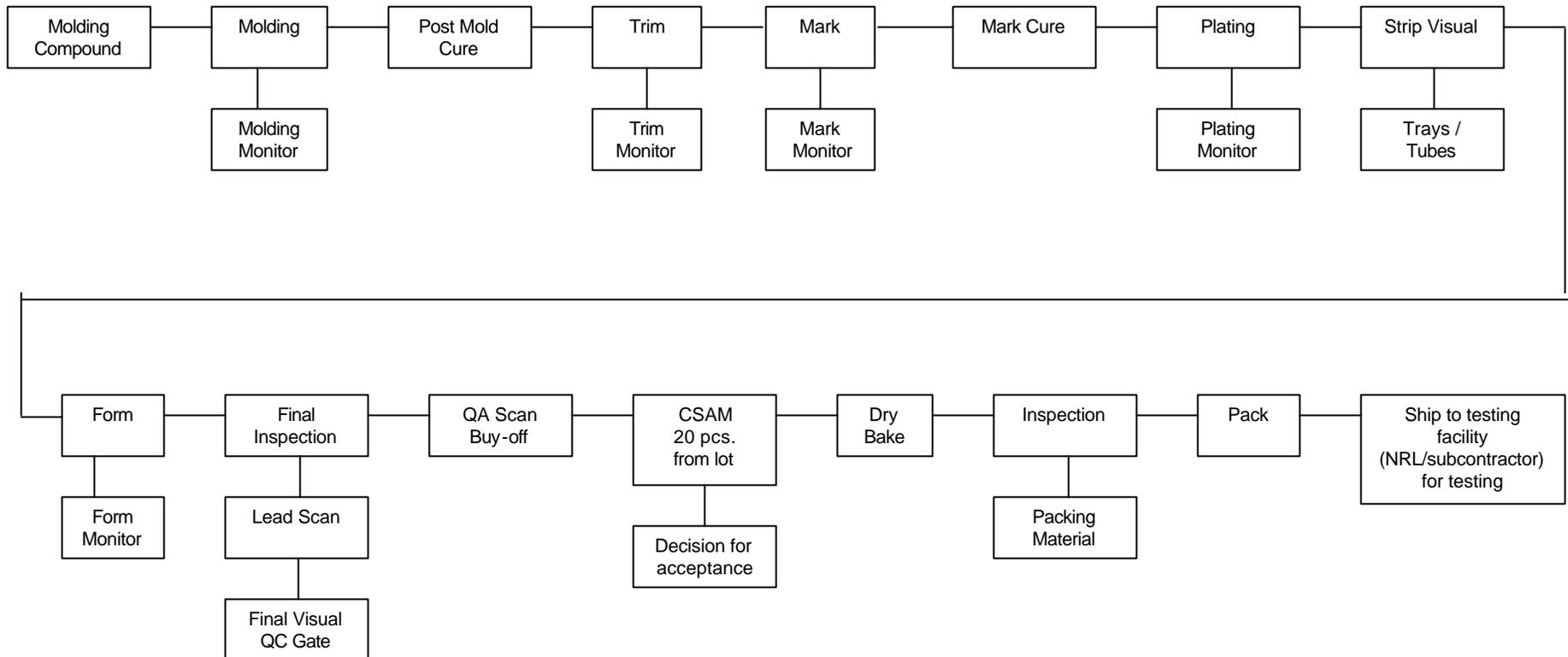


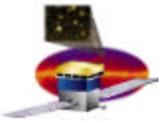
Process Flow Chart for ASICs





Process Flow Chart for ASICs

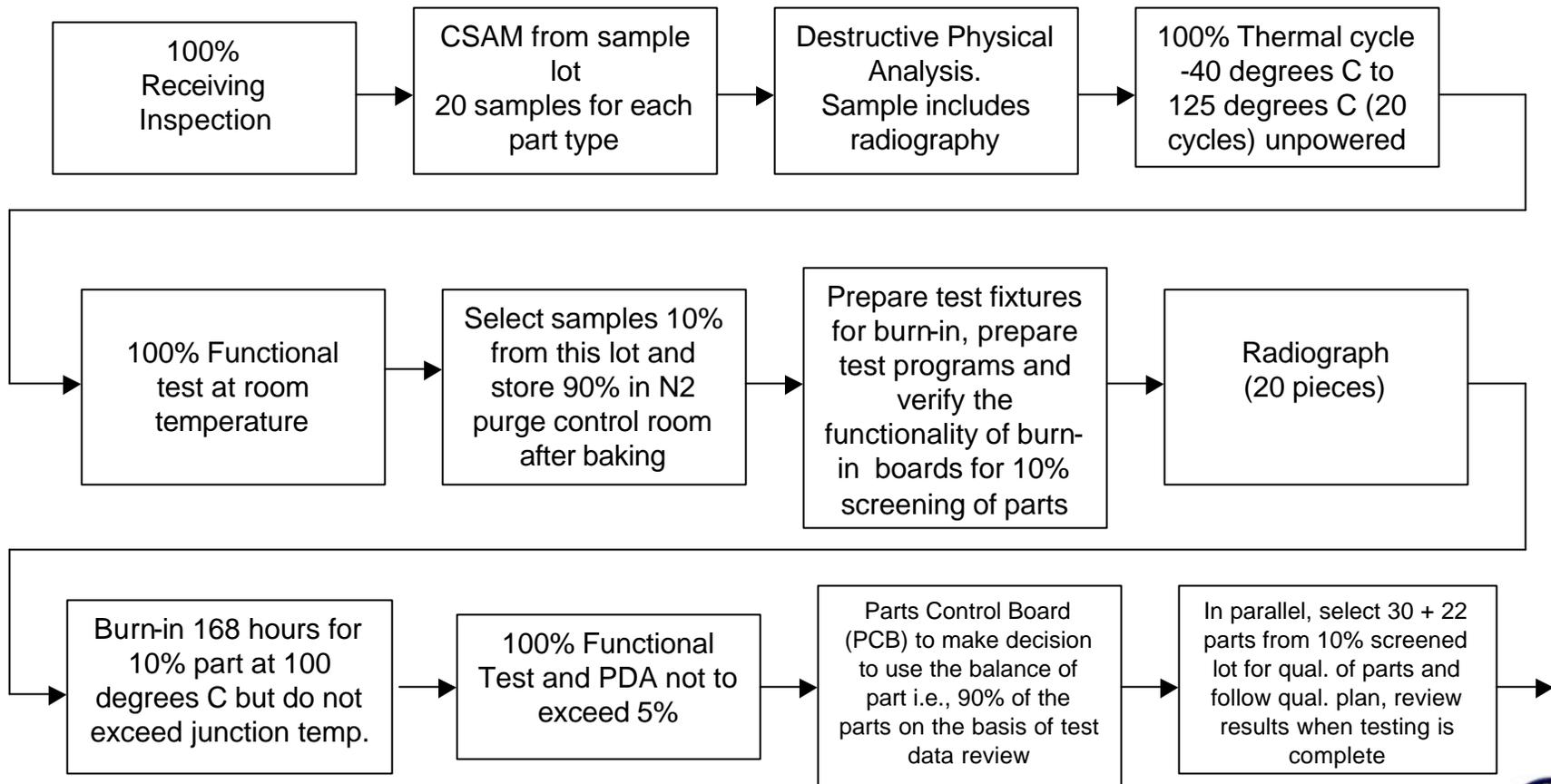


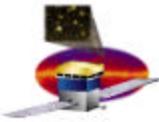


PEM (ASICs, ADC, DAC) Screening Flow

Single Wafer Lot and Single Manufacturing Lot

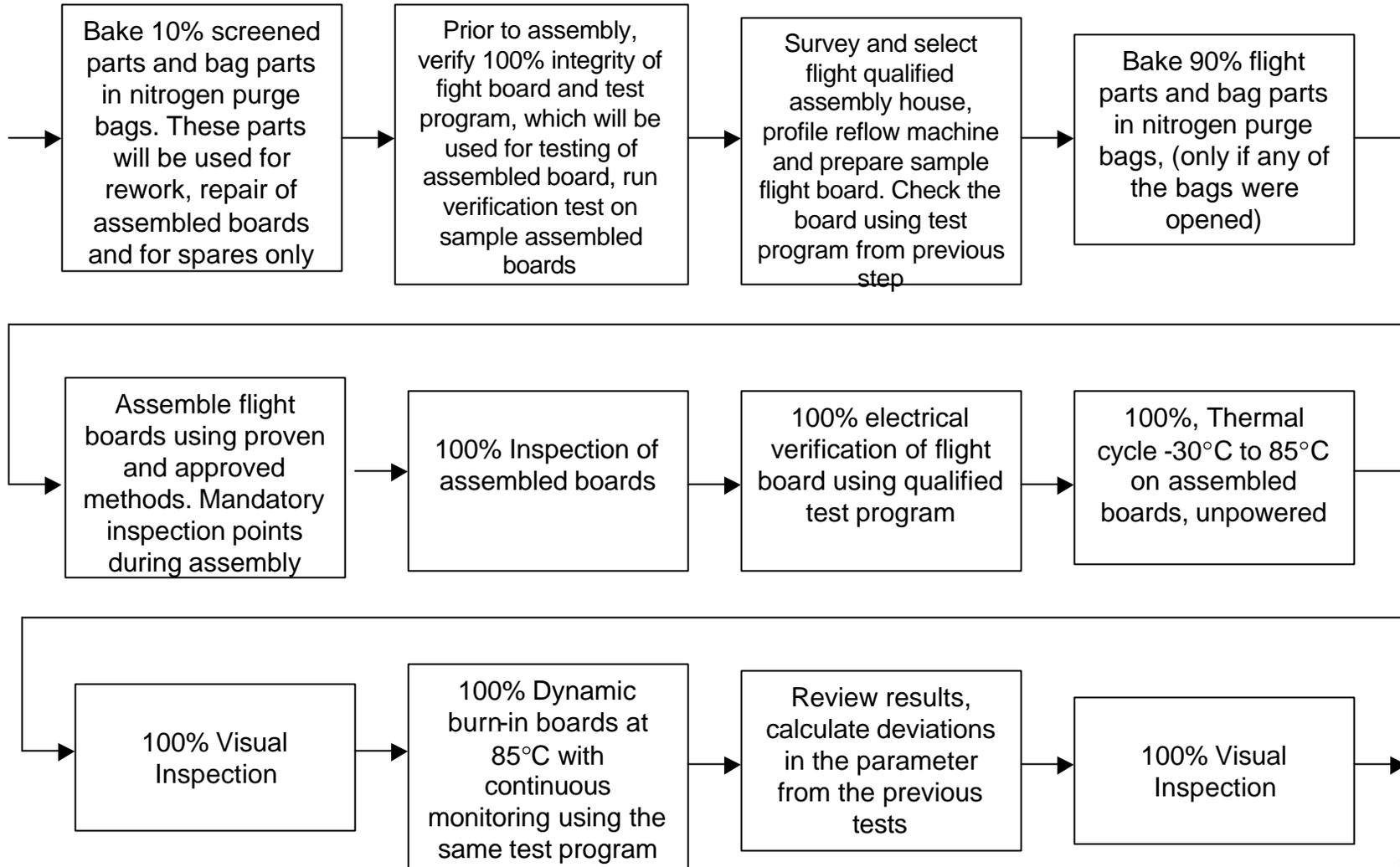
LAT instrument requirement Qual -30 degrees C to +50 degrees C, acceptance -10 to 30 degrees C, operational +25 degrees C, Radiation testing TID - 4.5K, SEE immune LET > 37 mev/mg/cm2, Humidity Control 30 to 45%, and 100% GSFC Parts Branch Involvement. 100% screening on 10% of lot size. Lot size should be > 200 pieces, otherwise perform screening on the entire lot.

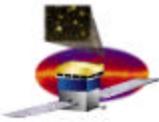




PEM (ASICs, ADC, DAC) Screening Flow

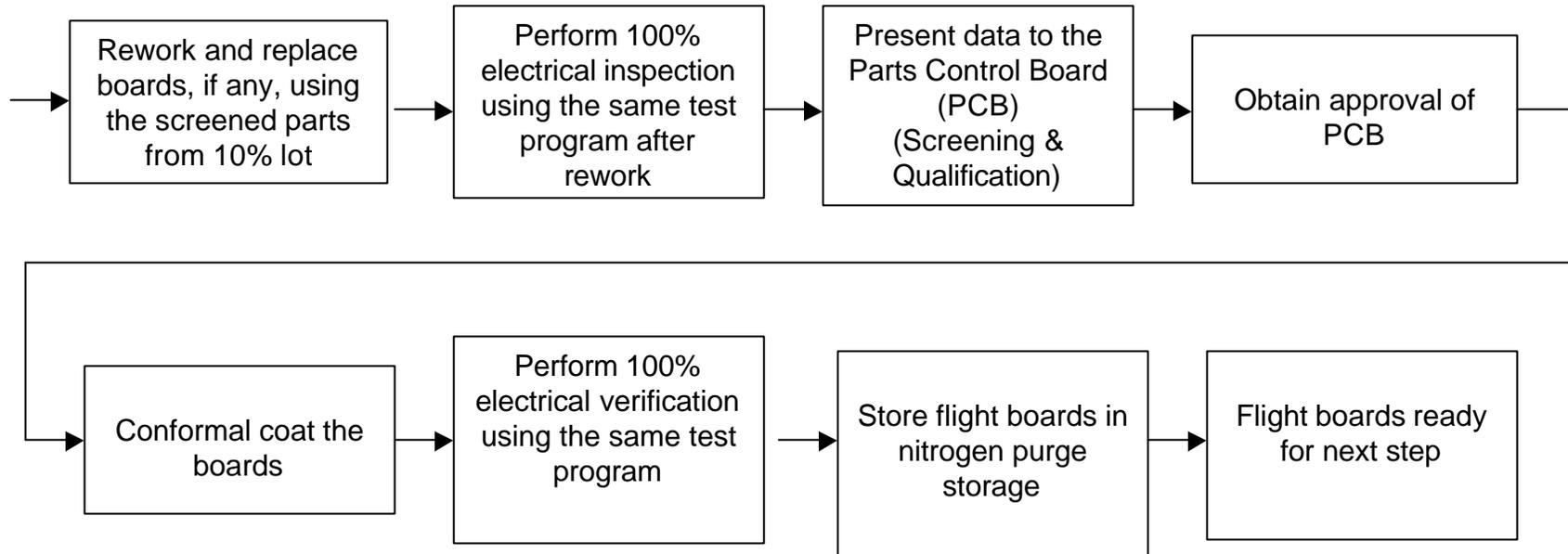
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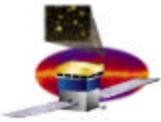




PEM (ASICs, ADC, DAC) Screening Flow

Single Wafer Lot and Single Manufacturing Lot

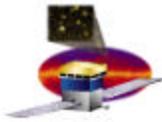




PEM Qualification on 30 + 22 Parts from Screened Lot

- **Preconditioning for moisture intake and reflow simulation (30pcs)**
- **Highly Accelerated Stress Test (HAST) (30pcs)**
 - **Unbiased HAST – 168 hrs at maximum temperature the part can operate and 85% RH**
 - **Electrical Testing at –30 degrees C, +25 degrees C, and +85 degrees C**
- **C-Mode Scanning Acoustic Microscope (CSAM) as per IPC/JEDEC, J-035 (15pcs)**
- **Destructive Physical Analysis (5pcs)**
- **Operation Life Test**
 - **As per MIL-STD-883, method 1005, condition D, 1000 hrs 22 pieces from flight screening lot**
 - **Electrical Testing**
 - **Review qualification report and data with Parts Control Board**

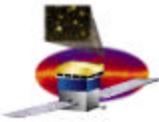




EEE Parts Concerns

- **ASICs**
 - Packaging of ASICs, screening, and qualification
 - Certify subcontractors for packaging, testing, and qualification
 - Radiation testing (TID, SEE, and SEU)
 - To mitigate risk, EM sample parts are being evaluated and do not expect any surprises
- **ADC & DAC**
 - Screening and qualification of Maxim parts and radiation testing
 - To mitigate risk, EM sample parts were evaluated and no anomalies were noticed

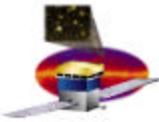




EEE Parts Concerns

- **2.5V Reference**
 - Radiation testing
 - Another 2.5V reference Rad-Hard part maybe considered to mitigate the risk
- **Connectors**
 - Due to the move and purchase of Nanonics connector from Arizona to California (New company called Microdot) the previous qualification is void. Working with the vendor to resolve issues related to qualification and screening
 - To mitigate risk, the vendor has been requested to submit generic Qual data for similar connectors
- **No outstanding issues**

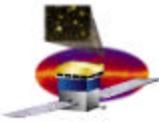




Radiation Testing

- All EEE parts are being reviewed by PCB and screened for radiation susceptibility against the radiation specification defined in GLAST 433-SPEC-0001
- Requirements:
 - Total dose requirement, including standard factor of 2 safety margin is 4.5 Krad (Si) for 5 years behind 100 mils Aluminum
 - Our goal is to test all parts up to 10 Krads (Si)
 - SEE Damage – no SEE shall cause permanent damage to the subsystem





Radiation Testing

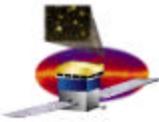
- **SEE Rate and Effects Analysis:**
 - **SEE rates and effects shall take place based on threshold LET (LET_{th}) as follows:**

<u>Device Threshold</u>	<u>Environment to be Assessed</u>
LET _{th} < 15 MeV*cm ² /mg	Cosmic Ray, Trapped Protons, Solar Heavy Ion and Proton
LET _{th} =15-37 MeV*cm ² /mg	Cosmic Ray, Solar Heavy Ion
LET _{th} > 37 MeV*cm ² /mg	No analysis required

SEE immune is defined as a device have an LET_{th} > 37 MeV*cm²/mg

- **Our goal is to test each part to this specification. In fact, all EEE parts susceptible to radiation will be tested for latch-up up to LET > 60 MeV*cm²/mg**

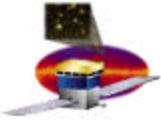




Radiation Testing Results

- Radiation testing was performed on engineering parts produced using similar processes and materials
- Maxim ADC and DAC were tested and met requirements
- An earlier version of ASIC tested and met requirements
- PIN Photodiode tested for total dose and met mission requirements with no degradation
- Crystal logs tested for total dose and met mission requirements
- Radiation testing of flight parts and plan:
 - All EEE parts will be tested to the previous requirements, in the USA
 - PIN Photodiodes will be tested in France to min. 10 Krads
 - Crystal logs will be tested in Sweden to min. 10 Krads
- No outstanding issues

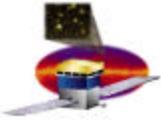




Electronic Packaging Program

- **Electronic Packaging, Manufacturing, Test, and Process Control program**
 - **Manufacturing, Assembly, and Quality Control of electronic system will be in compliance to the NASA technical standards: NASA-STD-8739.1, NASA-STD-8739.2, NASA-STD-8739.3, NASA-STD-8739.4, NASA-STD-8739.7, and IPC-6012 & 6013 or equivalent approved ESA standards**
- **Rigid PWBs shall meet the requirements of CAL AFEE Procurement Specification, LAT-DS-01127-01 based on Mil-PRF-55110F, IPC-6011 class 3, IPC-6012 class 3, and GSFC S-312-P-003 with a minimum internal annular ring of 0.002”**

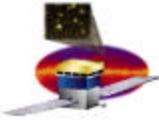




Electronic Packaging Program

- PWB Coupon will be analyzed by GSFC prior to flight assembly
- Particular attention will be paid to the quality of workmanship, soldering, welding, wiring, marking of parts and assemblies, plating and painting
- Verification of flight hardware will be performed by NASA certified and qualified personnel other than the original operator
- An item inspection will be performed on each component to verify:
 - Configuration is as specified on each component drawing/specification
 - Workmanship standards have been met
 - Test results are acceptable

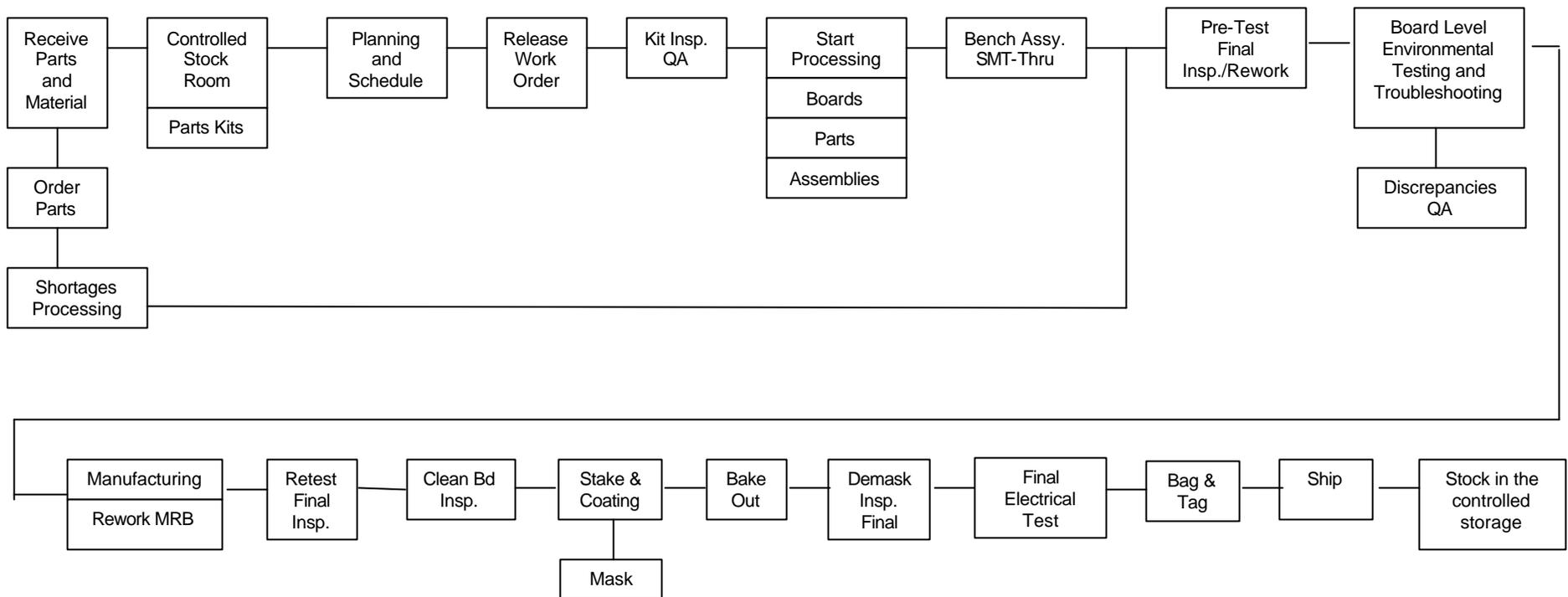


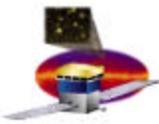


Electronic Packaging Program

Electronic Hardware Flow Process

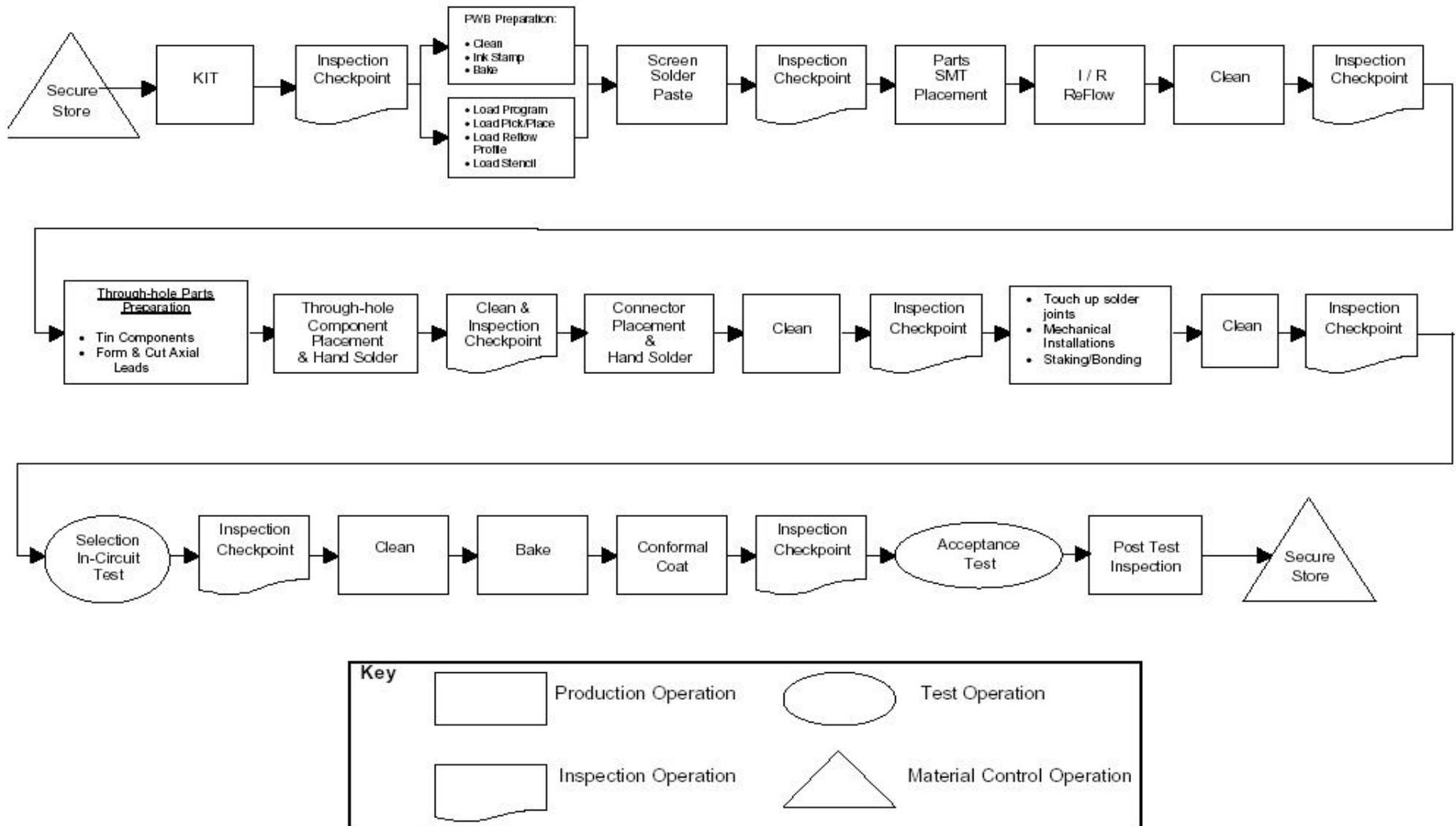
- All work will be performed using approved procedures

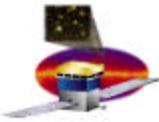




Electronic Packaging Program

Manufacturing and Process Control Flow Diagram of SMT PWB Assembly of AFEE Card





Manufacturing and Test Process Flow for Calorimeter Hardware

