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Document Title **CAL Front End (GCFE) ASIC – Version 7 Test Report**		

GLAST LAT Calorimeter Front-End Electronics (GCFE) ASIC

Version 7 Test Report

Document Approval

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Change History Log

Revision	Effective Date	Description of Change

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Applicable Documents:

1. LAT-PS-00910-01, "GLAST CAL Analog Front-End (GCFE) ASIC Version 6 and 7 Characterization Test Procedure", Tammy Faulkner, January 30, 2002.

2. LAT-SS-00424-D2, "GLAST LAT Design Description of the GLAST Calorimeter Front-End Electronics (GCFE) ASIC (GCFE7 submission)", W. Neil Johnson and James Ampe, November 28, 2001.

3. LAT-SS-00424-D2, "GLAST LAT Design Description of the GLAST Calorimeter Front-End Electronics (GCFE) ASIC (GCFE5 submission)", W. Neil Johnson and James Ampe, November 28, 2001.

4. LAT-SS-00089-D2, "GLAST LAT GLAST Calorimeter Front-End Electronics (GCFE) ASIC Specification", W. Neil Johnson, January 10, 2001.

5. LAT-SS-00208-D2, "Calorimter Readout Control ASIC – Conceptual Design"

Test Description

This document gives the test results from the execution of the GCFE ASIC Version 7 Characterization Test Procedure as documented in item 1. This test exercises the functionality and evaluates the performance of the ASIC chip. Where possible, the functionality of individual sub-devices on the ASIC are exercised and verified. Complete data acquisition sequences are performed to confirm end-to-end functionality and to verify those sub-devices that cannot be individually tested. Finally, Energy Range, Noise, and Linearity measurements are made as a measurement of performance.

The testing was performed on NRL's GCFE test board 2. All tests were performed with the nominally defined Pre-Amp Gain settings of LE = 5, HE = 13, unless otherwise stated. The complete test data and results can be found in the executed test procedure and accompanying spreadsheets. These spreadsheets will be kept on-file on the NRL server.

Test Summary:

	LEX8		LEX1		HEX8		HEX1	
	Expected	**Measured**	**Expected**	**Measured**	**Expected**	**Measured**	**Expected**	**Measured**
Shaper Output Noise, using Am-249 source & EM Diode				662 e-				1,045 e-
Track and Hold Output Noise, using Am-249 source & EM Diode		760 e-		1,936 e-		1,141 e-		2,633 e-
ADC Sampled Track and Hold Noise, using Calib. Strobe (1-sigma), No Input Capacitance.	< 2000 e-	1164 e- 2.16 mV	< 2000 e-	1806 e- 0.42 mV	< 2000 e-	9980 e- 1.76 mV	< 2000 e-	15,000 e- 0.38 mV
Integral Non-linearity	+/- 0.5%	+/- 0.3% for most chips	+/- 0.5%	+/- 0.3% for most chips	+/- 0.5%	+/- 0.3% for most chips	+/- 0.5%	+/- 0.2% for most chips
Signal Pedestal (ADC Reading for Cal DAC = 0)	100 mV	2.9 - 188 mV	100 mV	80 – 131 mV	100 mV	2.9 – 245 mV	100 mV	78 – 143 mV
Threshold Internal Trigger				14.6 mV 23.9 MeV				9.7 mV 1077 MeV
Energy Range Upper Limit	200 MeV	185 MeV	1.6 GeV	1.56 GeV	12.8 GeV	12.2 GeV	100 GeV	116 GeV
Fast Shaper Trigger Delay	0.5 +/- 0.2 μsec	0.5 +/- 0.2 μsec			0.5 +/- 0.2 μsec	0.5 +/- 0.2 μsec		
Slow Shaper Time to Peak (μsec)	3.5 +/-0.5 all w/i +/- 0.2		3.5 +/- 0.5 all w/i +/- 0.2	3.7 μsec	3.5 +/- 0.5 all w/i +/- 0.2		3.5 +/- 0.5 all w/i +/- 0.2	3.8 μsec
Preamp Gains	See table2							
Track and Hold Droop		< 1 LSB		< 1 LSB		< 1 LSB		< 1 LSB
Overload Recovery	Spec: < 100 μsec up to LEX8 x1000 (200,000 MeV)				Meas: 120 μsec, note glitch for some Energy Ranges			
Power Consumption	Spec: < 6 mW				Meas: 10.4 mW			

Chip Functionality:

All basic functionality was successfully verified. This included:

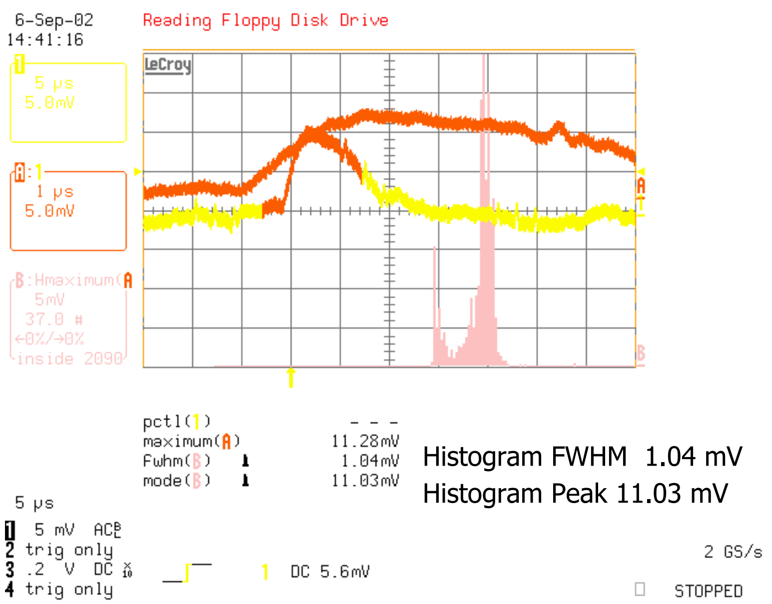
- Write and Read to all registers and DACs.
- Auto-Range transitions between each range
- Commanding of Pre-Amp gain settings.
- Internal Triggering
- Track and Hold of shaped Signal

Noise Measurements:

Scope Measurements:

GCFE ver 7 Shaper and track and hold output noise measurements using LeCroy oscilloscope and AM-249 source directly into EM diodes.

Figure 1 LE shaper pulse height histogram with Am-249 source.



LE Shaper FWHM = 1.04 mV, Peak 11.03 mV, Baseline 0mV (AC coupled probe), 16,500 electrons/photon in silicon.
LE Shaper Noise sigma = (1.04 mV FWHM / 2.35 FWHM/sigma) * (16,500 e- / 11.03 mV) = 662 electrons.

Figure 2 LEx1 track and hold histogram with Am-249 source.

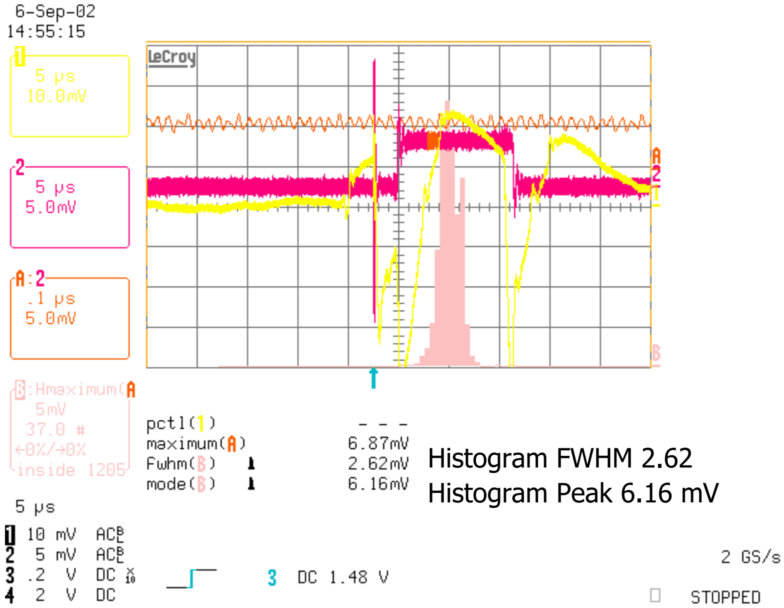
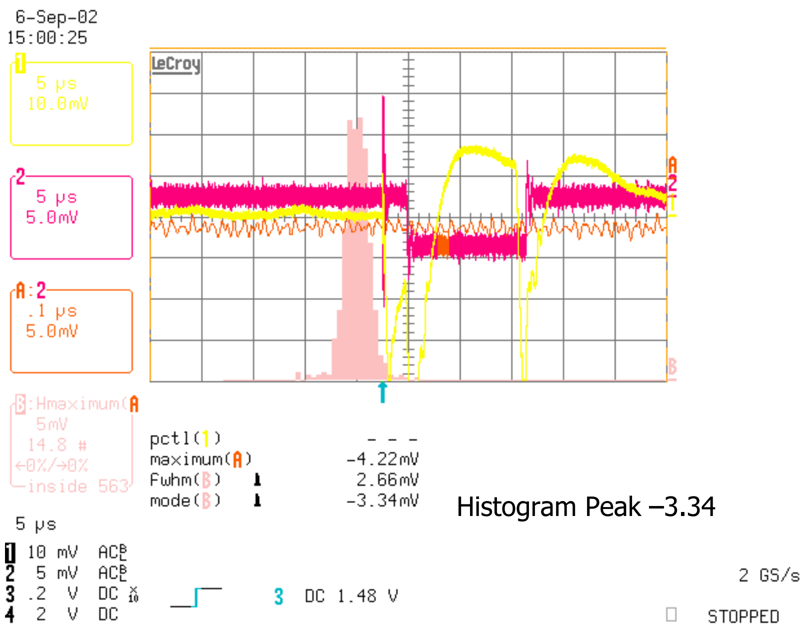


Figure 3 LEx1 track and hold baseline.



Lex1 FWHM = 2.62 mV, Peak 6.16 mV, Baseline –3.34mV, 16,500 electrons/photon in silicon.
Lex1 Noise sigma = (2.62 mV FWHM / 2.35 FWHM/sigma) * (16,500 e- / (6.16- -3.34 mV)) = 1,936 electrons.

We noticed that the Lex1 track and hold output can vary between two states as shown in Figure 4 below. This has been noted in previous GCFE versions. The shaper output amplitude does not change. The shift is slow in time. Do not know if it is gain shift or charge injection shift.

Figure 4 Example of LEx1 track and hold output shift.

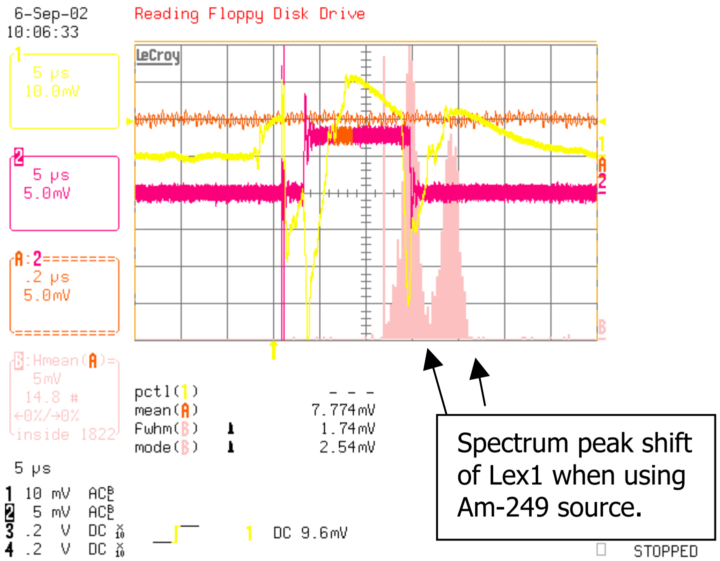


Figure 5 LEx8 track and hold histogram with Am-249 source.

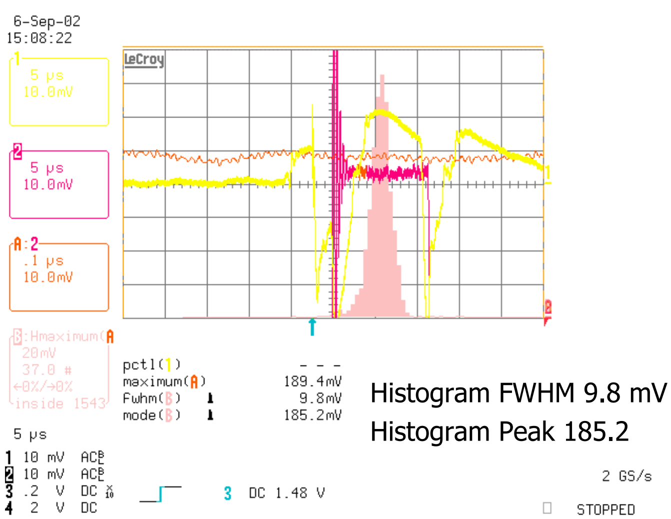
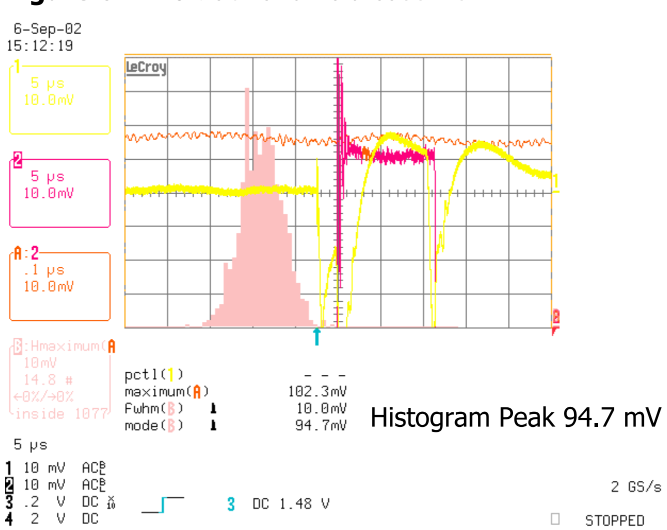
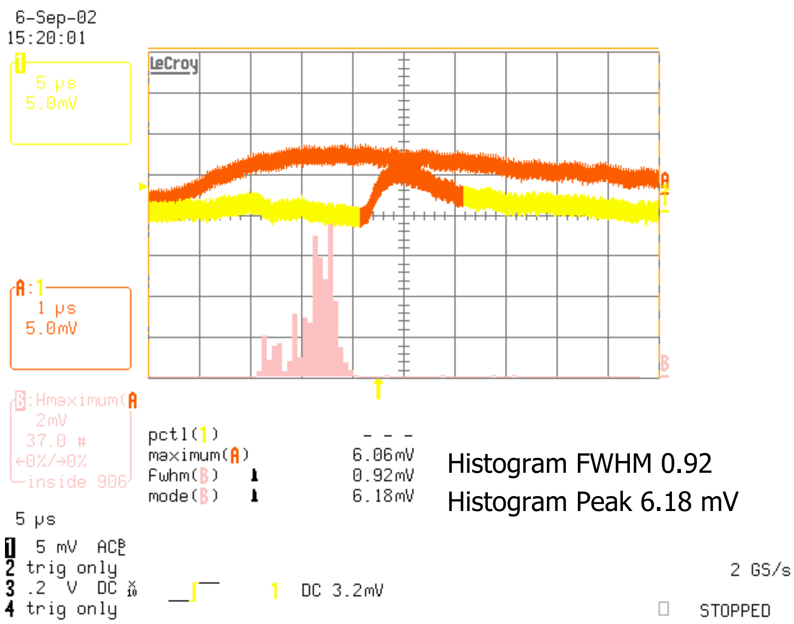


Figure 6 LEx8 track and hold baseline.



Lex8 FWHM = 9.8 mV, Peak 185.2 mV, Baseline 94.7mV, 16,500 electrons/photon in silicon.
Lex8 Noise sigma = (9.8 mV FWHM / 2.35 FWHM/sigma) * (16,500 e- / (185.2– 94.7 mV)) = 760 electrons.

Figure 7 HE shaper pulse height histogram with Am-249 source.



HE shaper FWHM = 0.92 mV, Peak 6.18 mV, Baseline 0mV (AC coupled probe), 16,500 electrons/photon in silicon.
HE shaper Noise sigma = (0.92 mV FWHM / 2.35 FWHM/sigma) * (16,500 e- / 6.18 mV) = 1,045 electrons.

Figure 8 HEx1 spectrum with Am-241 source.

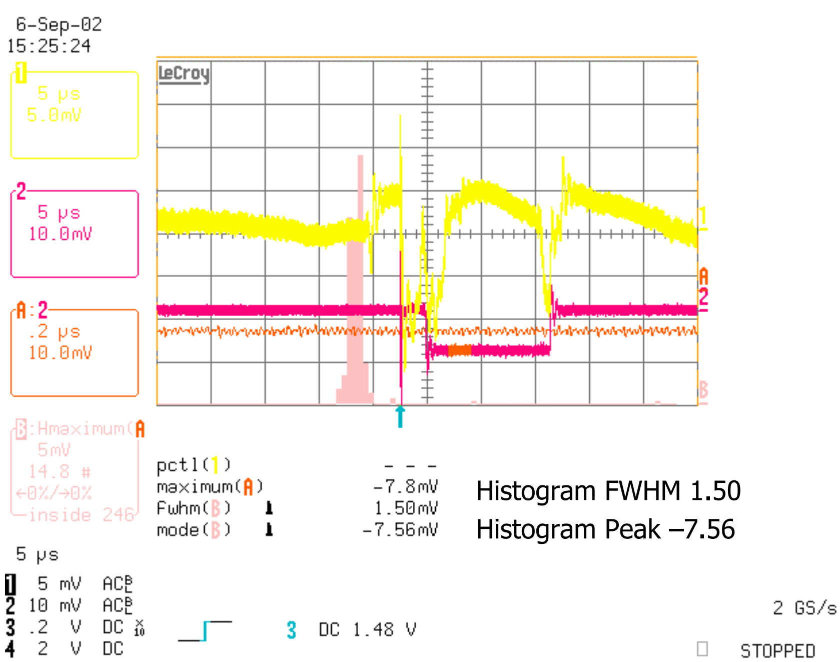
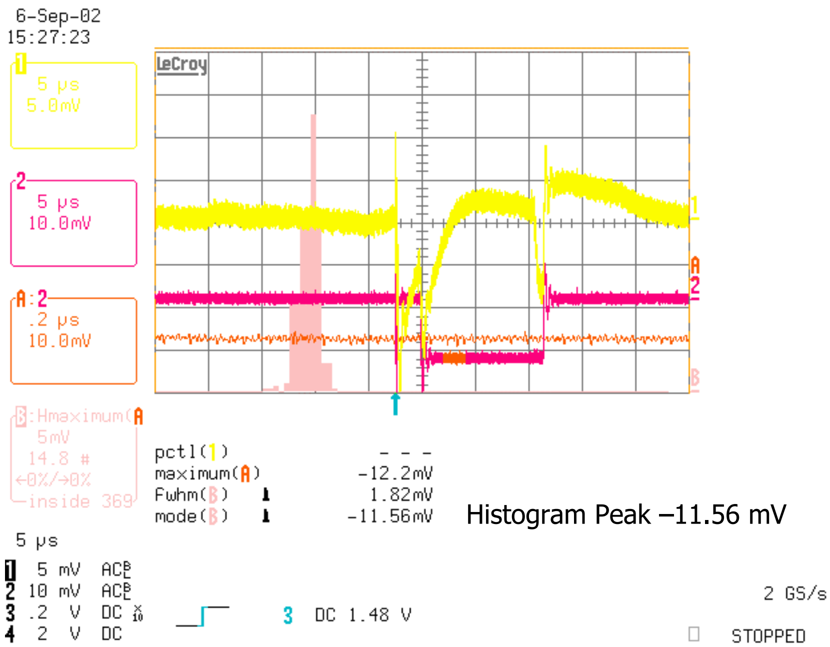


Figure 9 HEx1 track and hold baseline.



Hex1 FWHM = 1.5 mV, Peak –7.56 mV, Baseline –11.56 mV, 16,500 electrons/photon in silicon.
Hex1 Noise sigma = (1.5 mV FWHM / 2.35 FWHM/sigma) * (16,500 e- / (-7.56 - -11.56 mV)) = 2,633 electrons.

Figure 10 HEx8 spectrum with Am-241 source.

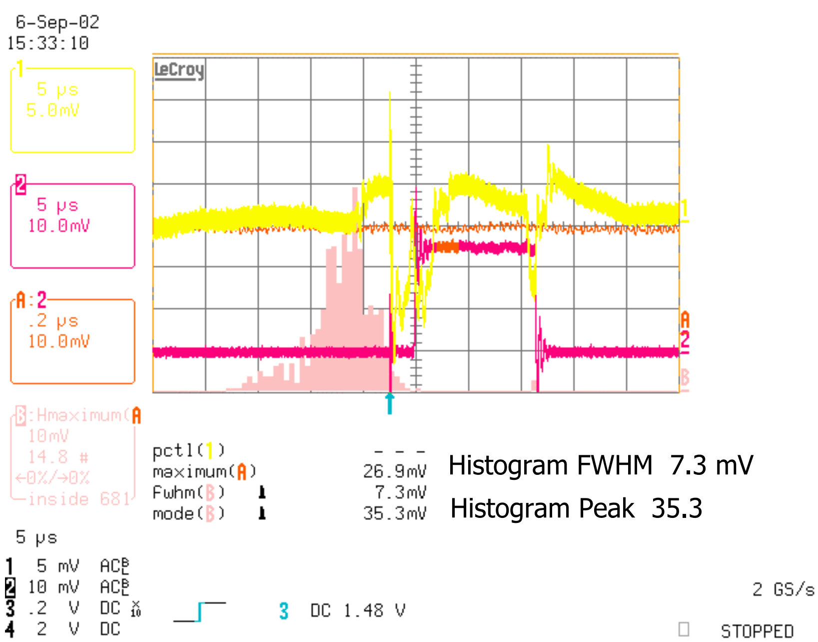
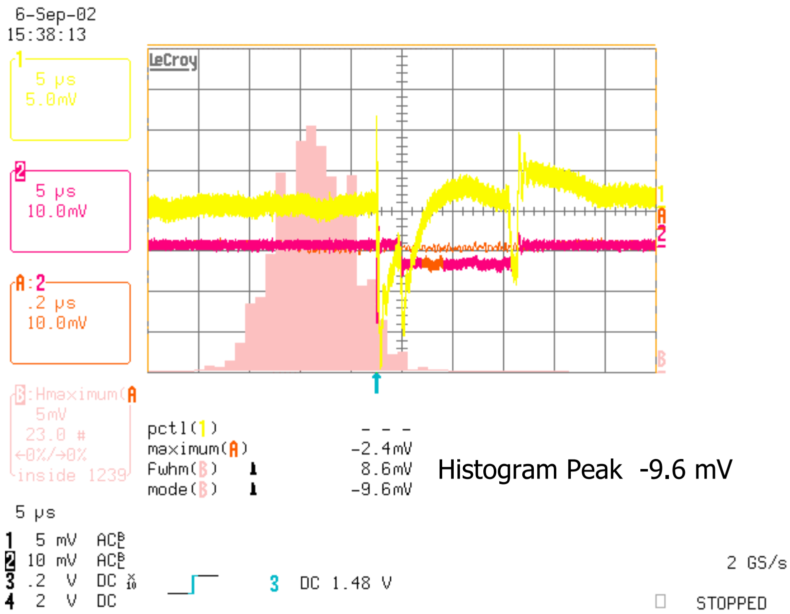


Figure 11 HEx8 track and hold baseline.



Hex8 FWHM = 7.3 mV, Peak 35.3 mV, Baseline –9.6 mV, 16,500 electrons/photon in silicon.
Hex8 Noise sigma = (7.3 mV FWHM / 2.35 FWHM/sigma) * (16,500 e- / (35.3 - -9.6 mV)) = 1,141 electrons.

Functional Test Noise Results:

Measurements were made using the GCFE calibration input and the MAX 145 ADC to read the analog output signal. The measurements were made in a minimal noise environment with the test board enclosed in a metal box without scope probes or other sources of noise.

The calibration DAC was stepped 64 steps over its range with 120 measurements taken at each step. The mean and standard deviation of each step were recorded to a spreadsheet. Once the ADC reading exceeds 2300 mV, the pre-determined saturation point, the recording of measurements stop. The measurements in mV are then converted to MeV using the procedure and equations documented in appendix A.

The results in mVolts show that the LEX1 and HEX1 noise standard deviation is within 1 LSB of the resolution of the 12-bit ADC, while the LEX8 and HEX8 channels are 3-4 LSB.

Figure 12: GCFEv7 Noise using ADC, (1-sigma)

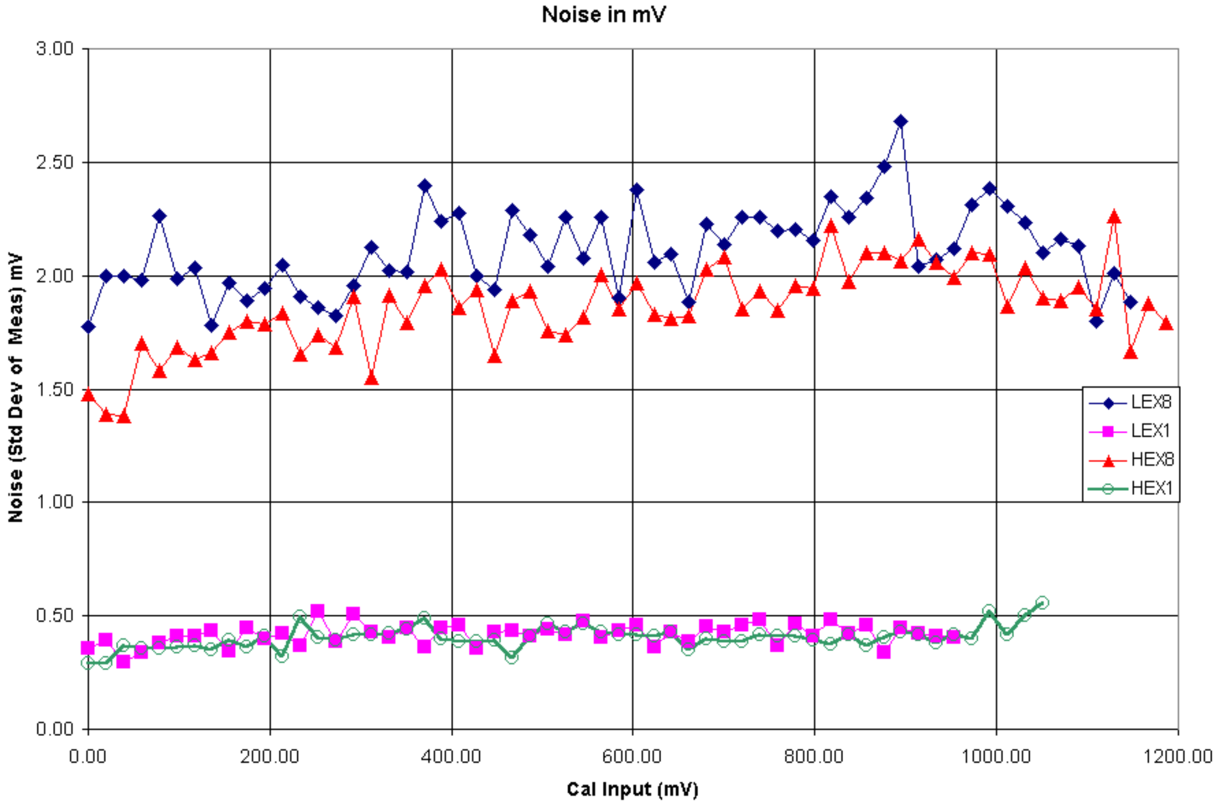
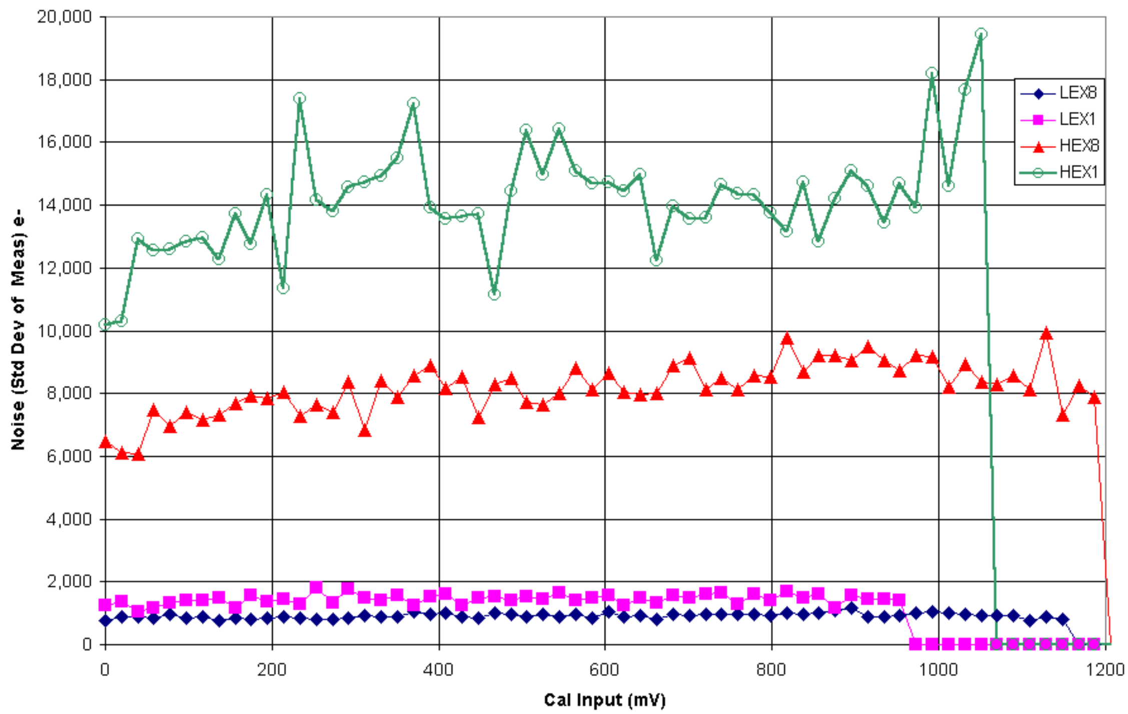


Figure 13 GCFEv7 Noise using ADC, Referred to Input electrons (1-sigma)



As shown in Figure 13, when referred to the input, the high-energy channel noise greatly exceeds the low energy channel noise. From Figure 12 the output noise of the high energy channel is similar to the output noise of the low energy channel, but the gain of the high energy channel is a factor of 8 -10 less. Thus the input referred noise of the high-energy channel is about 8 times higher than that of the low energy channel.

The functional testing was then repeated on the batch of plastic packaged ASICs. Note that the increase in noise on some chips was repeatably observed during multiple test runs with the same chip, yet was also noticed to be absent during other test runs. To this point, a correlation for the cause of the noise has not been found.

Figure 14 Compilation of LEx1 noise from 14 GCFE chips.

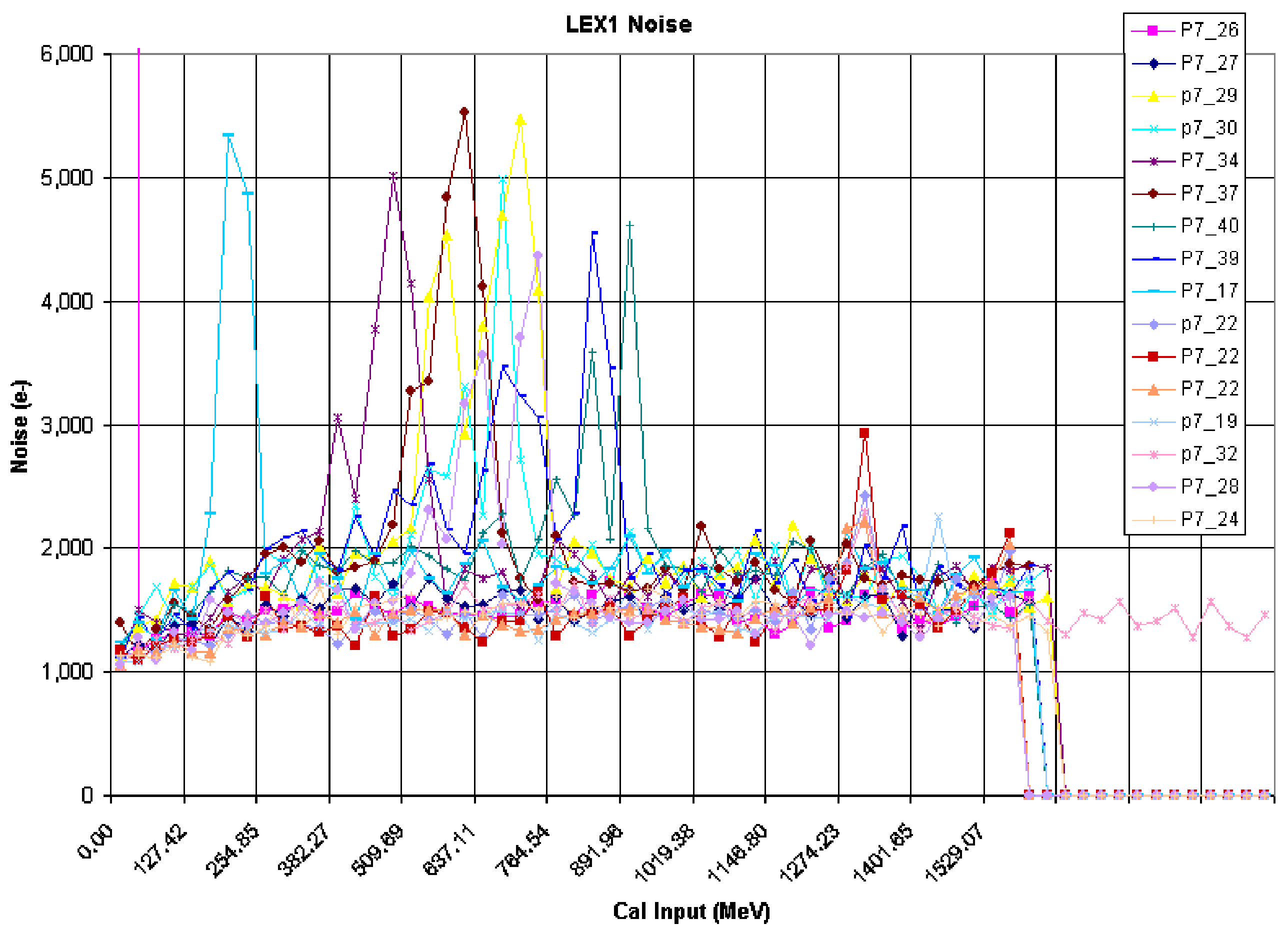


Figure 15 Compilation of LEx8 noise from 14 GCFE chips.

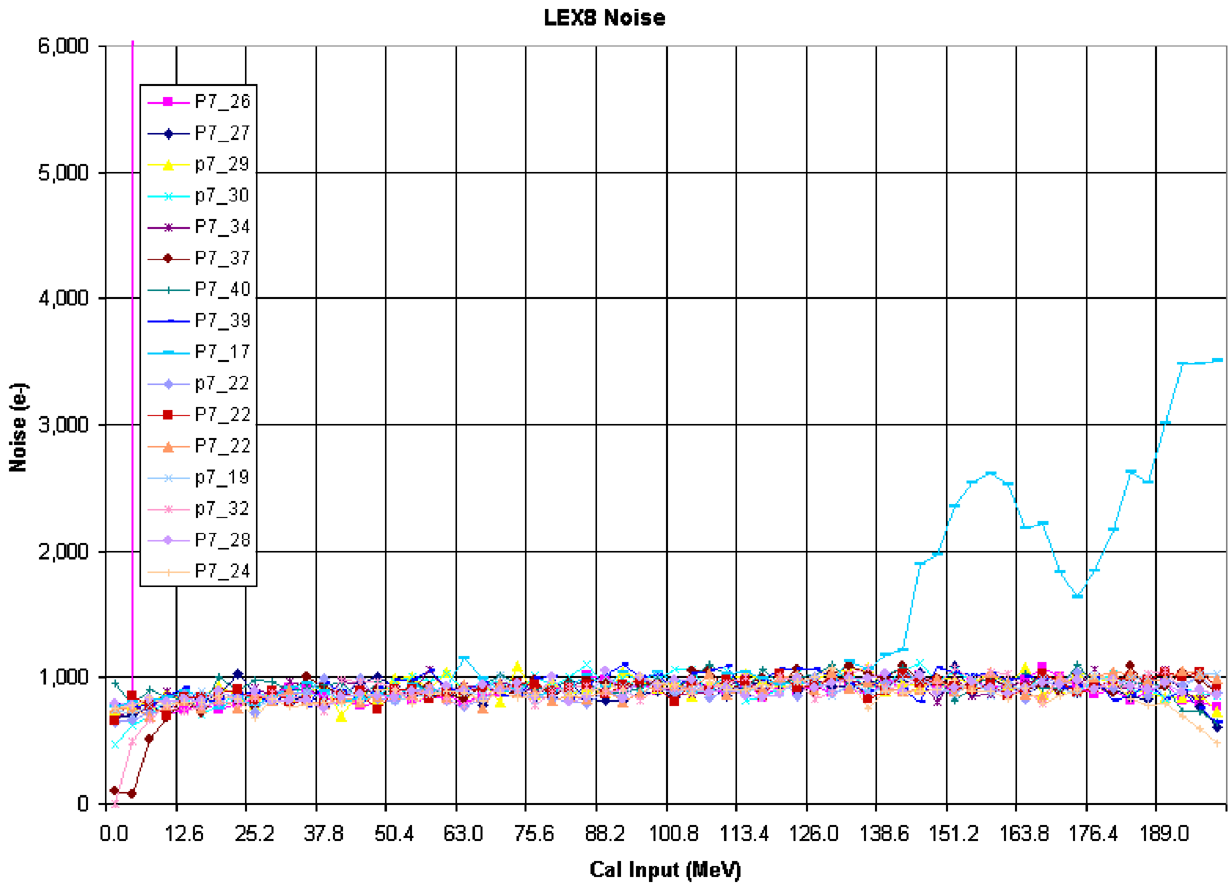


Figure 16 Compilation of HEx8 noise from 14 GCFE chips.

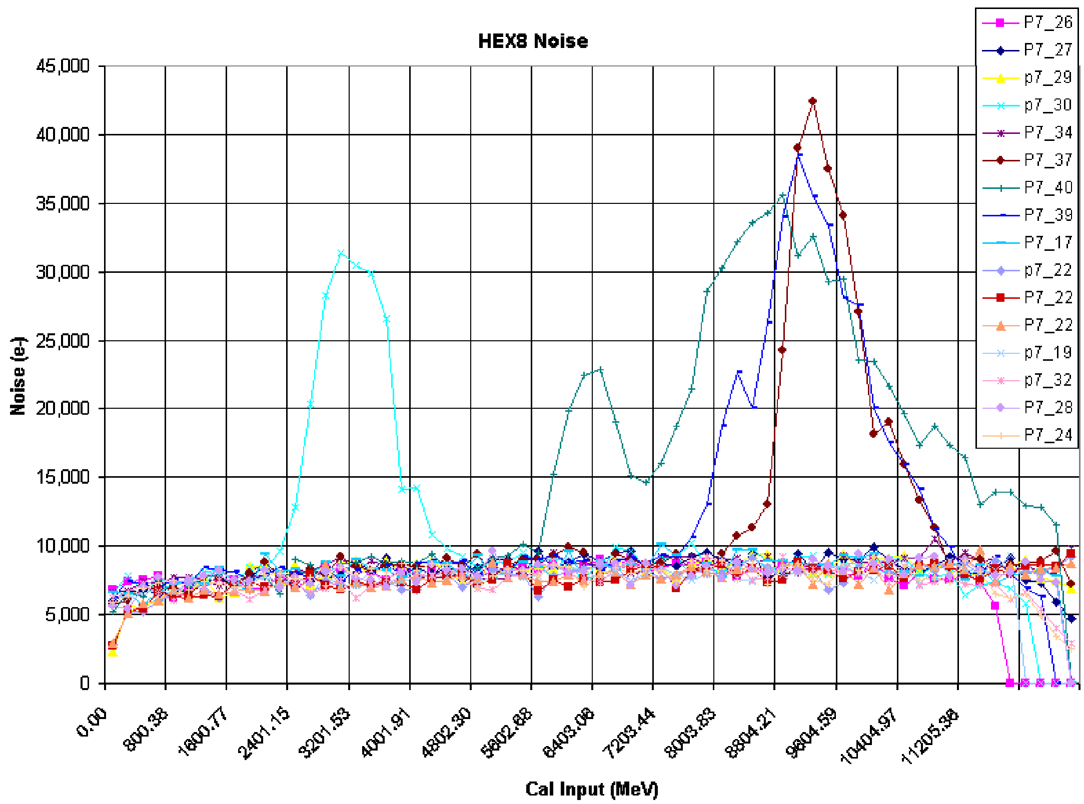
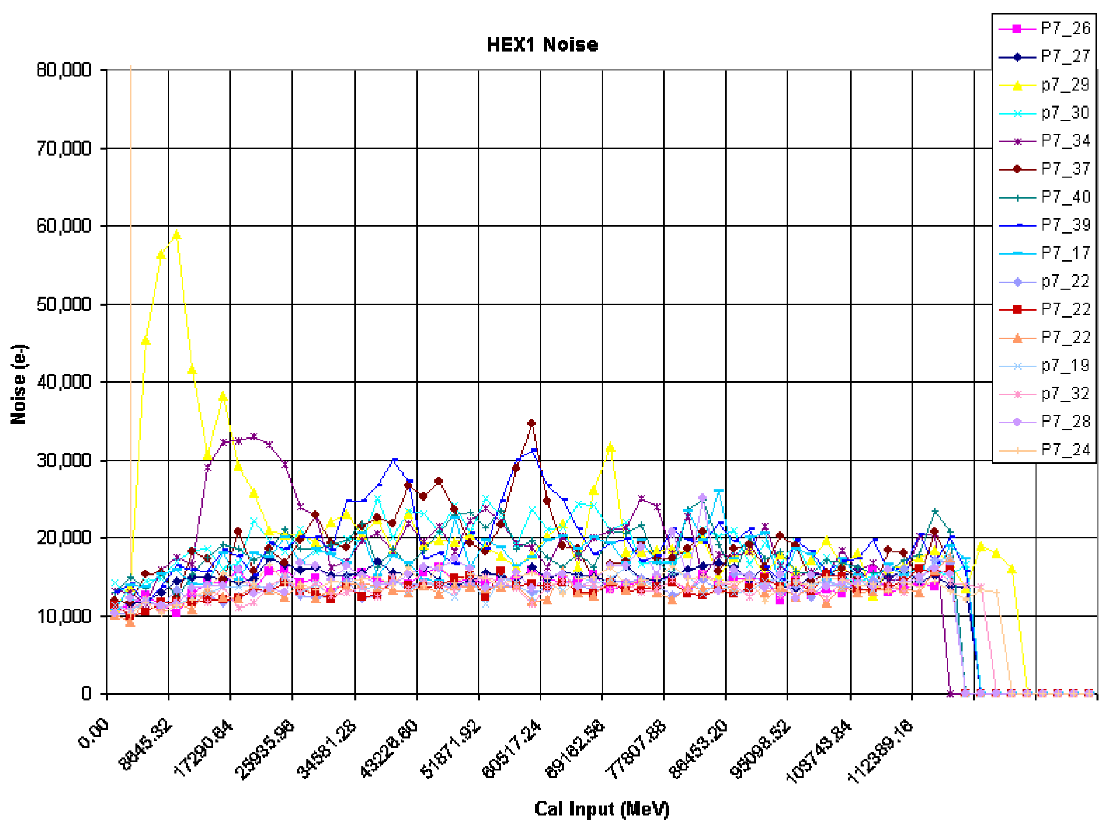


Figure 17 Compilation of HEx1 noise from 14 GCFE chips.



Integral Non-Linearity Measurements:

Integral Non-linearity measurements are calculated as difference from a least-squares fit. The percentage error of the measured value is the difference from the linear fit, divided by the measured Energy Range (maximum signal). The linearity is calculated over the range from 0 signal input through to just prior to saturation. This may include points under the intended threshold for that range. The specification is for the non-linearity is less than +/- 0.5 %.

Note that variations in the saturation voltages of the output signal were noticed to be lower in those chips with a lower pedestal value. The low saturation also translates to a sooner than expected loss of linearity. One of the better examples of this is chip 32, which has a LEX8 pedestal of 3 mV and saturates at 2230 mV, while normal saturation is at 2350 mV.

Figure 18 Compilation of LEx8 linearity measurements from 14 GCFE chips.

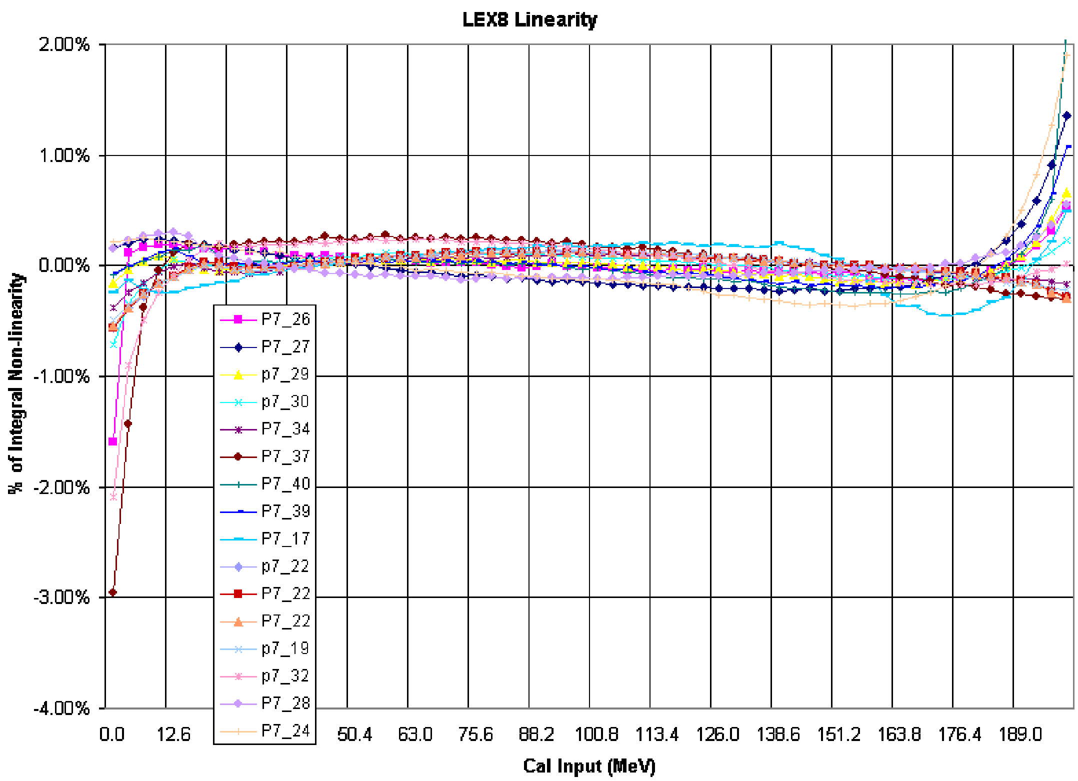


Figure 19 Compilation of LEx1 linearity measurements from 14 GCFE chips.

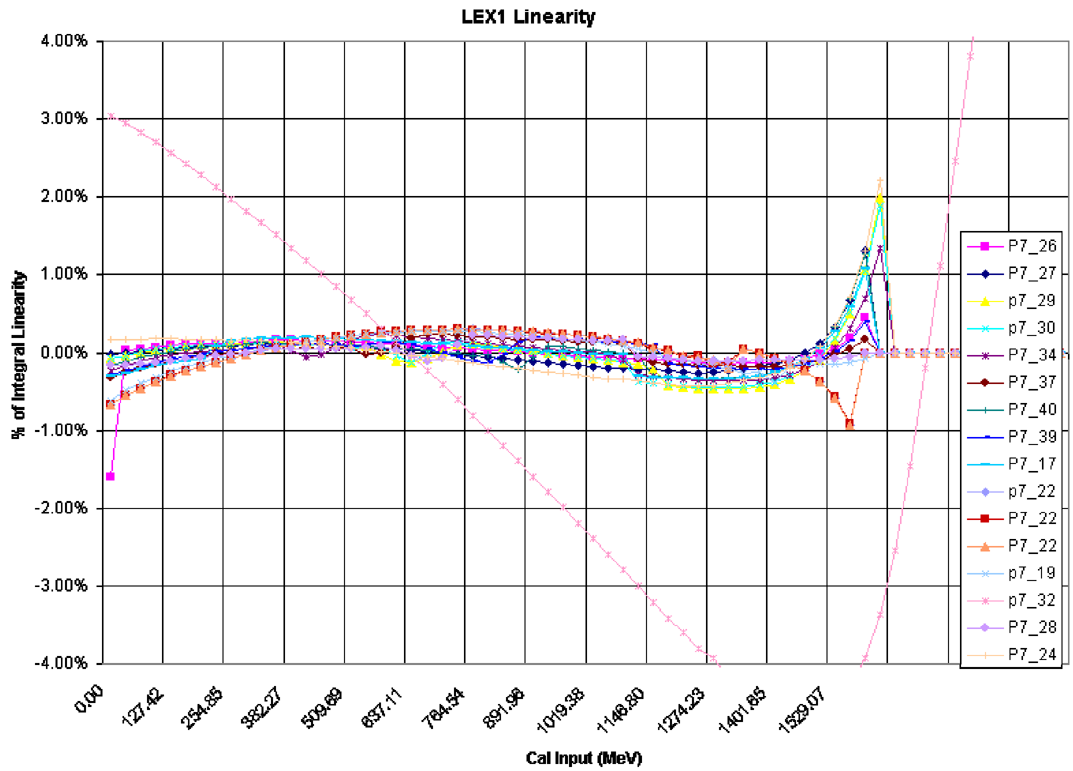


Figure 20 Compilation of Hex8 linearity measurements from 14 GCFE chips.

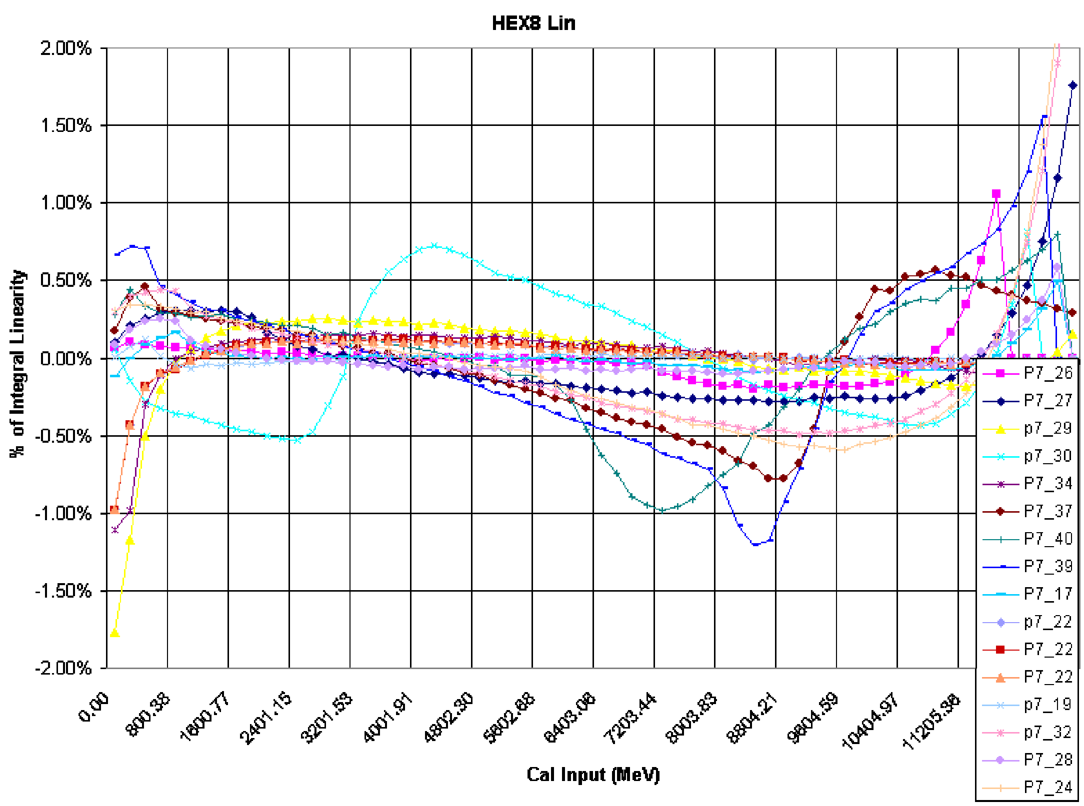
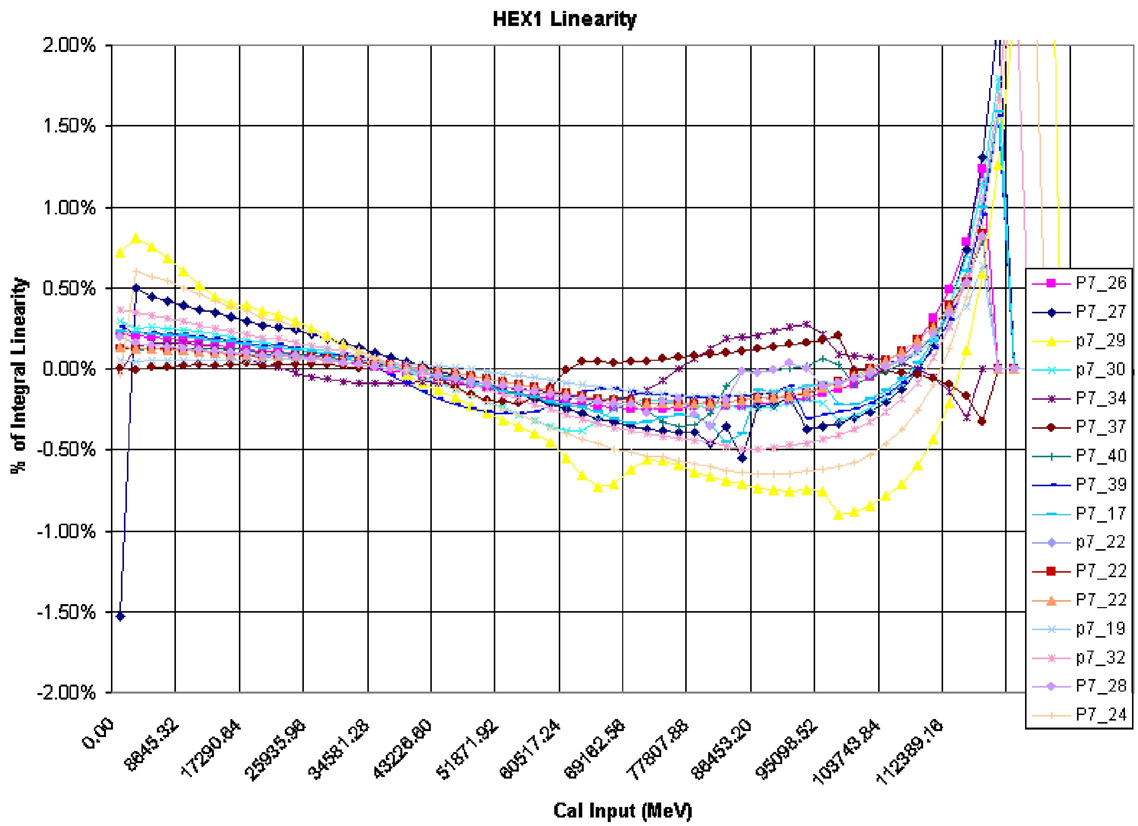


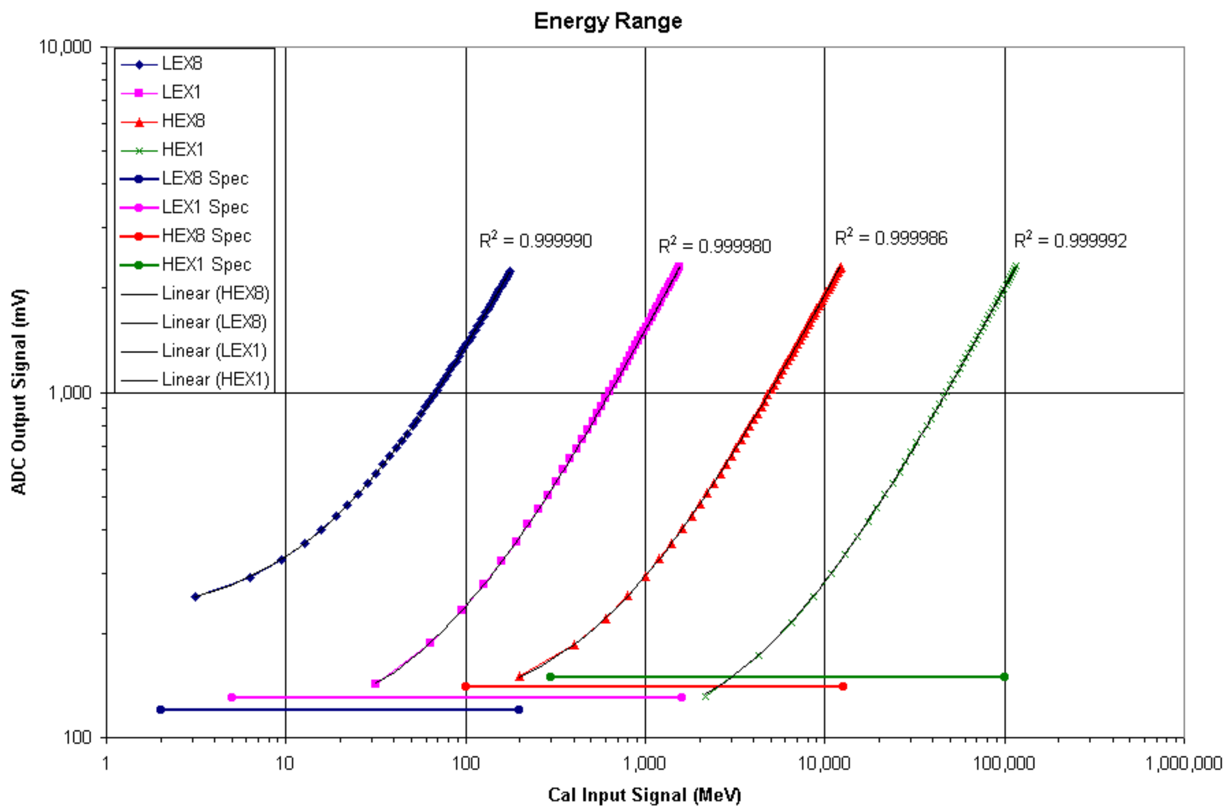
Figure 21 Compilation of HEx1 linearity measurements from 14 GCFE chips.



Energy Range:

The Energy Range measurements are shown in Figure 22. Note that these measurements are made with the test board commanded trigger, not with the internal trigger. The actual low-energy threshold will be higher since the DAC setting for the fast shaper trigger function must be set above the noise level to avoid triggering on non-pulse events.

Figure 22 Energy range of GCFE chip, measured and expected (expected are horizontal lines at bottom).



The energy range was then tested on a sampling of the plastic packaged chips. The largest chip-to-chip variation noticed was in the pedestal values of the LEX8 and HEX8 channels. They were measured to vary between 3.4 and 180 mV for identical testing from chip-to-chip. The following plots show this variation:

Figure 23 Compilation of LEx8 energy range measurements from 14 GCFE chips.

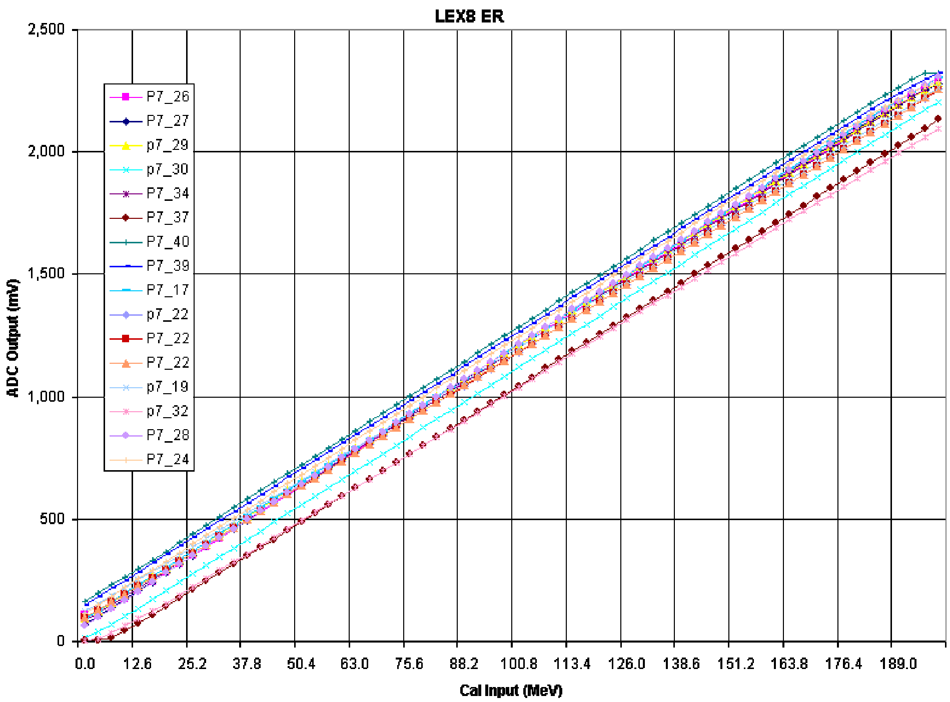


Figure 24 Compilation of LEx1 energy range measurements from 14 GCFE chips.

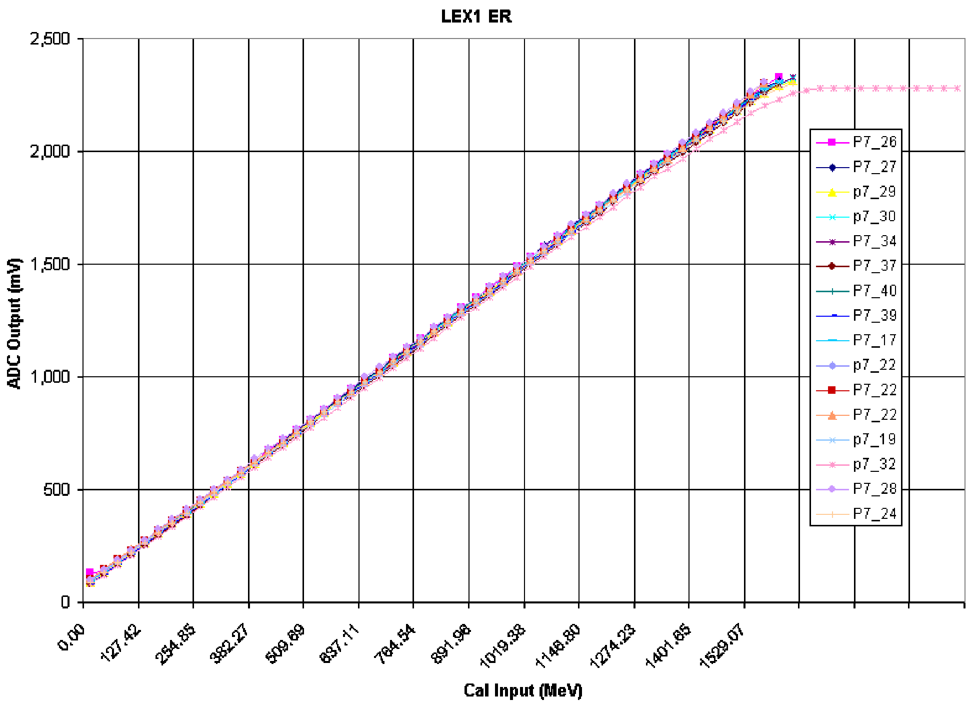


Figure 25 Compilation of HEx8 energy range measurements from 14 GCFE chips.

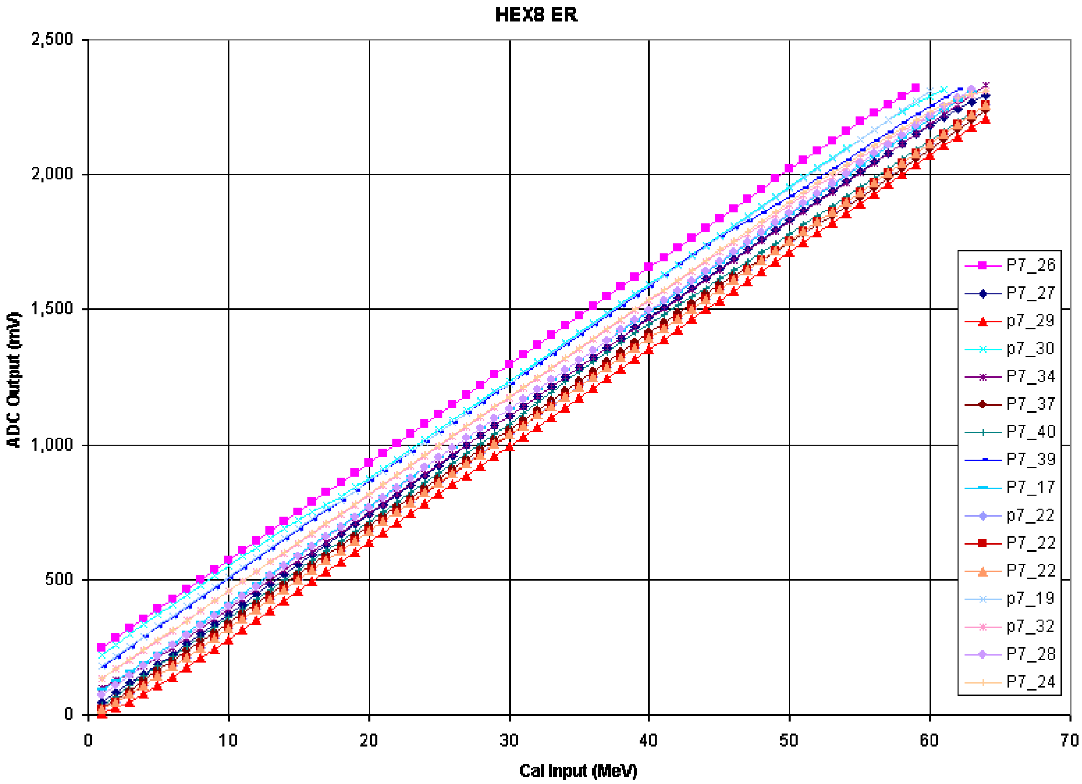
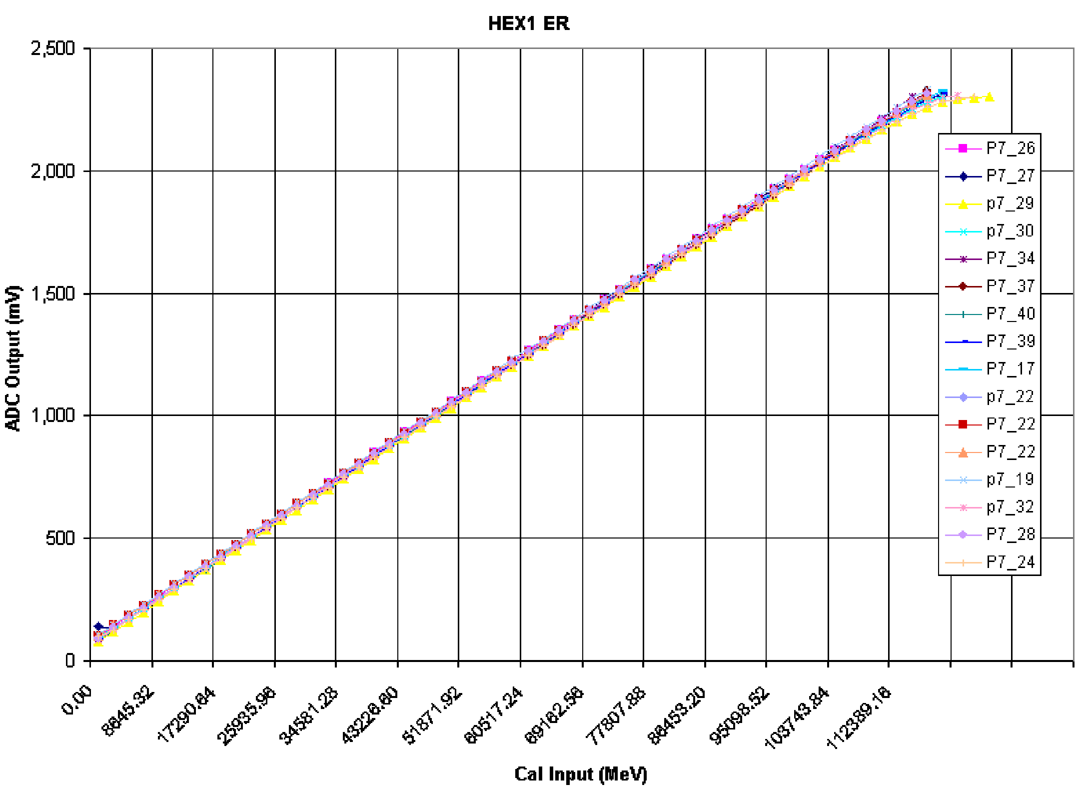


Figure 26 Compilation of HEx1 energy range measurements from 14 GCFE chips.



Fast Shaper Threshold Energy Range

It was determined that for most chips, the following fast shaper discriminator values allowed the lowest possible setting without false-triggering on noise:

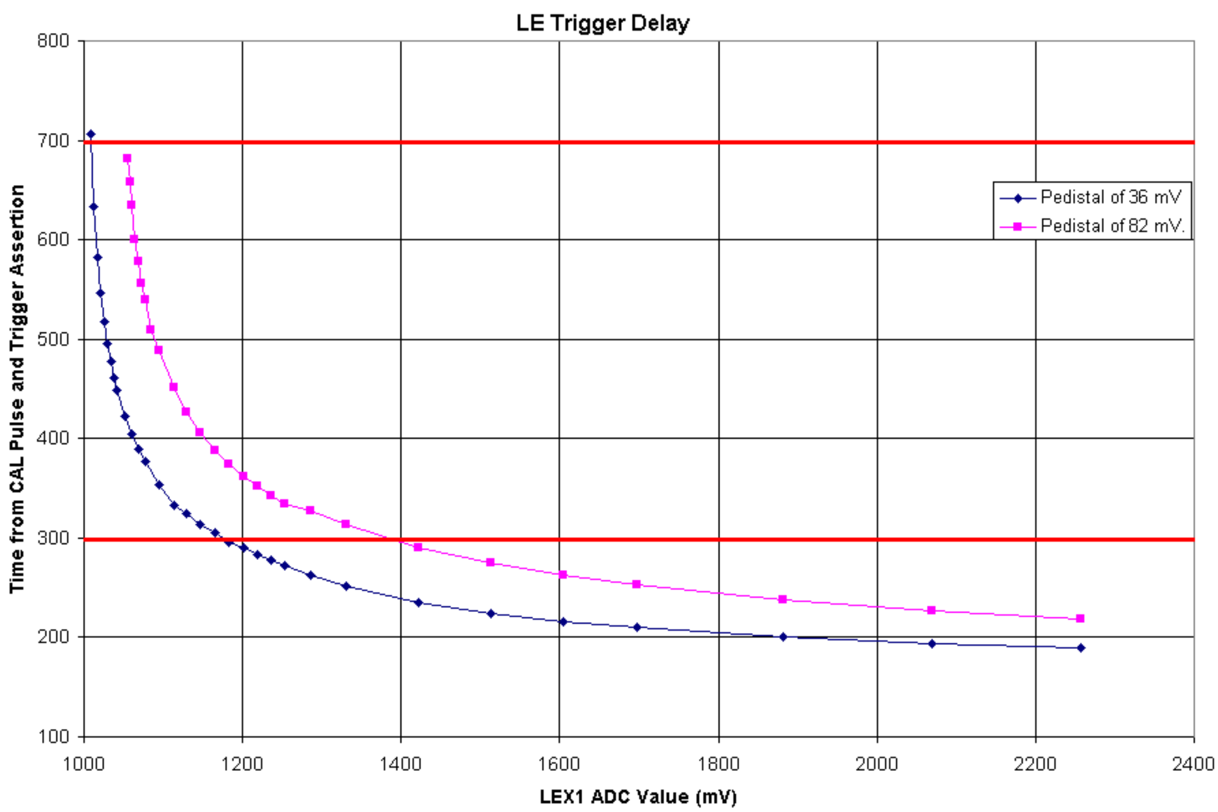
FLE_DAC = 9
FHE_DAC = 1

Measurements were made with the discriminator DACs setting at this level and repeatable. The LEX1 and HEX1 channel triggered with an input signal between 20-35 mV with less than 15 mV chip-to-chip variation.

Fast Shaper Trigger Delay

The time from the calibration strobe to the fast shaper discriminator transition was measured on a scope for the full range of input signals. Measurements for two different FLE_DAC settings were performed. The DAC settings were chosen as one low threshold voltage and one high threshold. The specification calls for the trigger delay time to be 0.5 +/- 0.2 usec for all chips. The time ranged from 0.70 μsec for small pulses to as fast as 0.19 μsec for large input pulses.

Figure 27: Low Energy Trigger Delay Measurements



Slow Shaper Peaking Time:

The slow shaper time-to-peak was measured for a sample of the chips for a single calibration signal input level. The LE time-to-peak varied between 3.63 and 3.78 usec. The HE time-to-peak varied from 3.80 to 3.95 usec. The results are shown in Table 1:

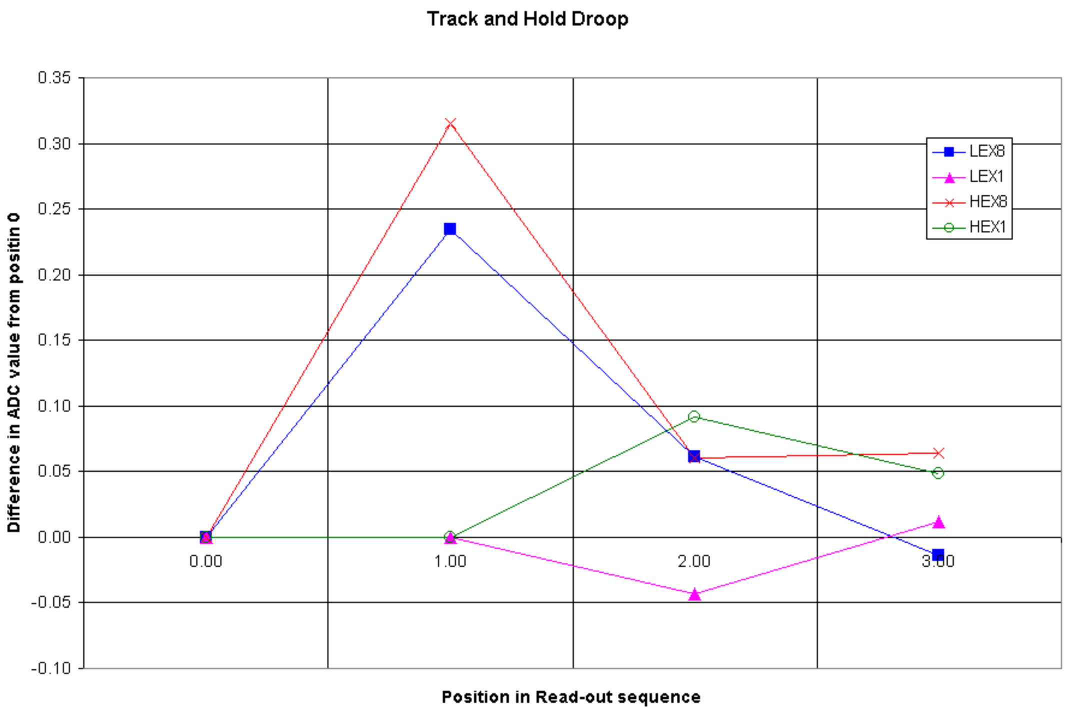
Table 1 Measured time-to-peak for 21 GCFE chips.

Chip ID	LE Shaper Time to Peak (usec)	HE Shaper Time to Peak (usec)
p7_0	3.67	3.80
p7_7	3.78	3.96
p7_9	3.75	3.86
p7_10	3.67	3.82
p7_11	3.67	3.84
p7_20	3.64	3.83
p7_22	3.74	3.87
p7_24	3.76	3.92
p7_25	3.74	3.89
p7_26	3.74	3.86
p7_27	3.74	3.83
p7_28	3.73	3.83
p7_29	3.77	3.93
p7_30	3.76	3.90
p7_31	3.73	3.95
p7_32	3.76	3.86
p7_33	3.77	3.86
p7_34	3.63	3.76
p7_35	3.75	3.92
p7_36	3.75	3.88
p7_37	3.71	3.95

Track and Hold Droop:

Measurements were taken in the GCFE 4-range readout mode, alternating the readout order. Comparison of the ADC values of the same range, between different readout order, gives a measurement of the droop of the held signal. The resulting measurements in Figure 28, show droop to be less than 1 LSB of the ADC (0.6 mV).

Figure 28 GCFE track & hold droop measured by alternating readout order.



Gains Measurements:

Gains are measured as slope of the graphed input calibration signal vs. output X1 channel ADC value. Gains were measured for each of the 16 GCFE preamp gain selections. The expected normalized gain values are computed from "GCFE v7 Design Documentation" tables 9 and 12. The results in Table 2 show that the measured normalized gain is very close to the design goal.

Table 2 GCFE gain measurements of shaper outputs.

	Shaper output measured normalized gain LEX1	**Expected normalized gain LE**	**Shaper output measured normalized gain HEX1**	**Expected normalized gain HE**
Gain State 0	2.96	3.04	10.52	10.65
Gain State 1	2.13	2.15	4.39	4.38
Gain State 2	1.65	1.67	2.76	2.76
Gain State 3	1.26	1.36	1.83	2.01
Gain State 4	1.17	1.16	1.61	1.59
Gain State 5	1.00	1.00	1.30	1.30
Gain State 6	0.87	0.88	1.13	1.11
Gain State 7	0.78	0.79	0.96	0.97
Gain State 8			3.04	3.04
Gain State 9			2.17	2.16
Gain State 10			1.61	1.67
Gain State 11			1.30	1.37
Gain State 12			1.17	1.15
Gain State 13			1.00	1.00
Gain State 14			0.87	0.88
Gain State 15			0.78	0.79

Logic Accept Discriminator Verification:

Functionality and noise of the Logic Accept Discriminator was measured for three GCFE chips. For the following plots the internal calibration pulser is used at fixed external DAC setting and the resulting Lex1 ADC data values are graphed along with the log accept bit value from each event. The noise in the log accept bit values is the intersection of the log accept bit '0' distribution with the log accept bit '1' distribution. The width of the log accept noise, or uncertainty, is approximately 7 ADC bits of the Lex1 range, for the three chips tested.

Figure 29 Log accept measurement, GCFE P7_59, DAC setting 1E6h.

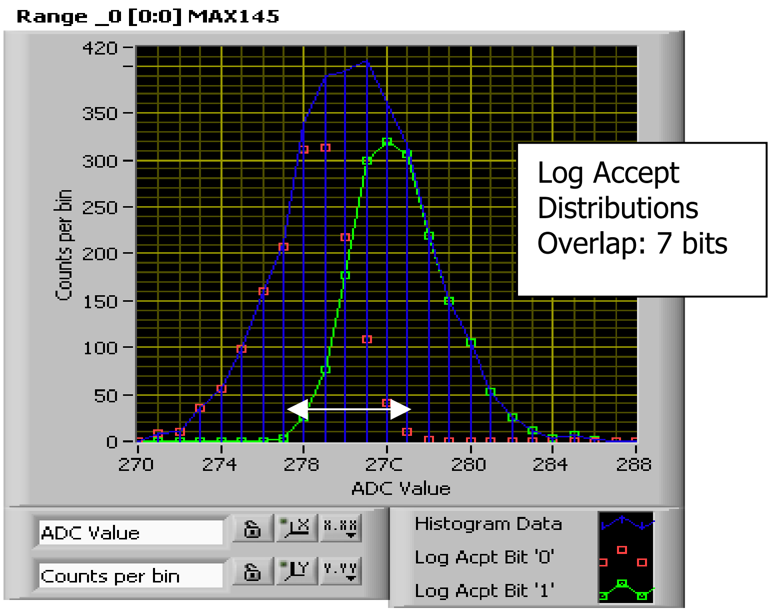


Figure 30 Log accept measurement, GCFE P7_58, DAC setting 26Ah.

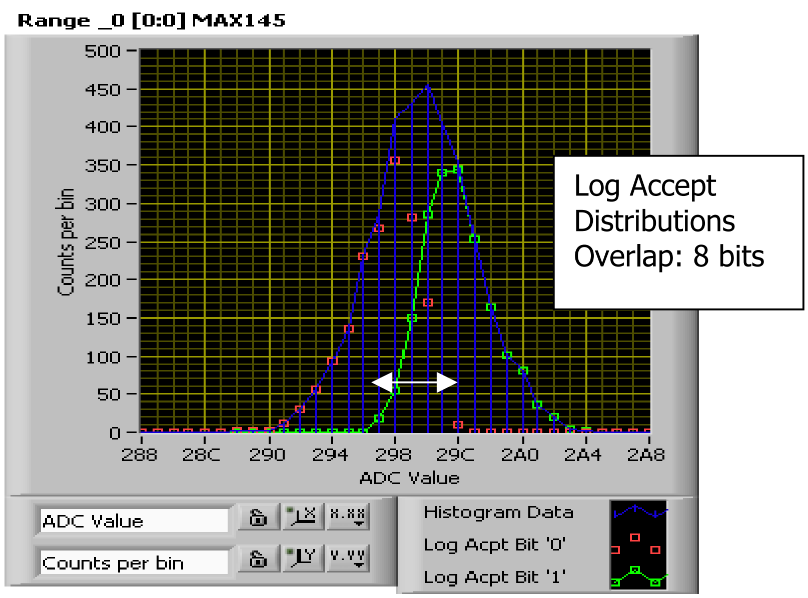
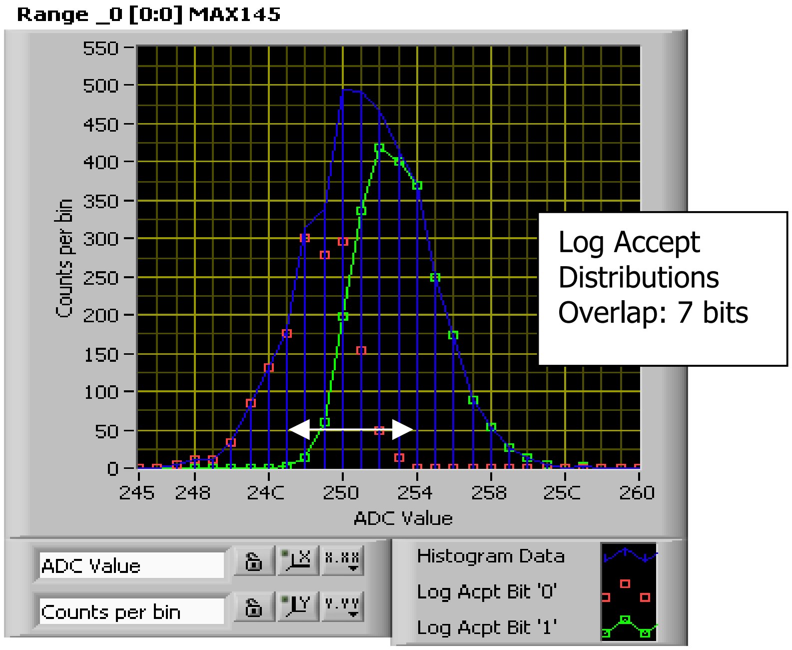
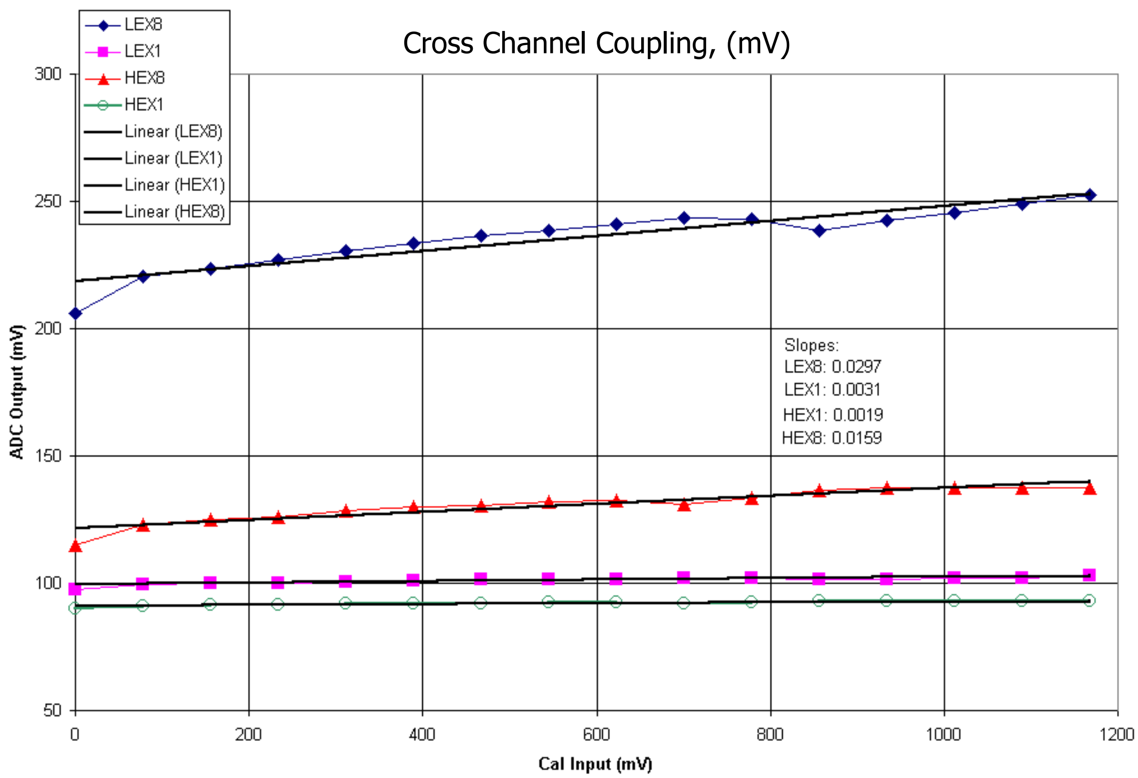


Figure 31 Log accept measurement, GCFE P7_57, DAC setting 156h.



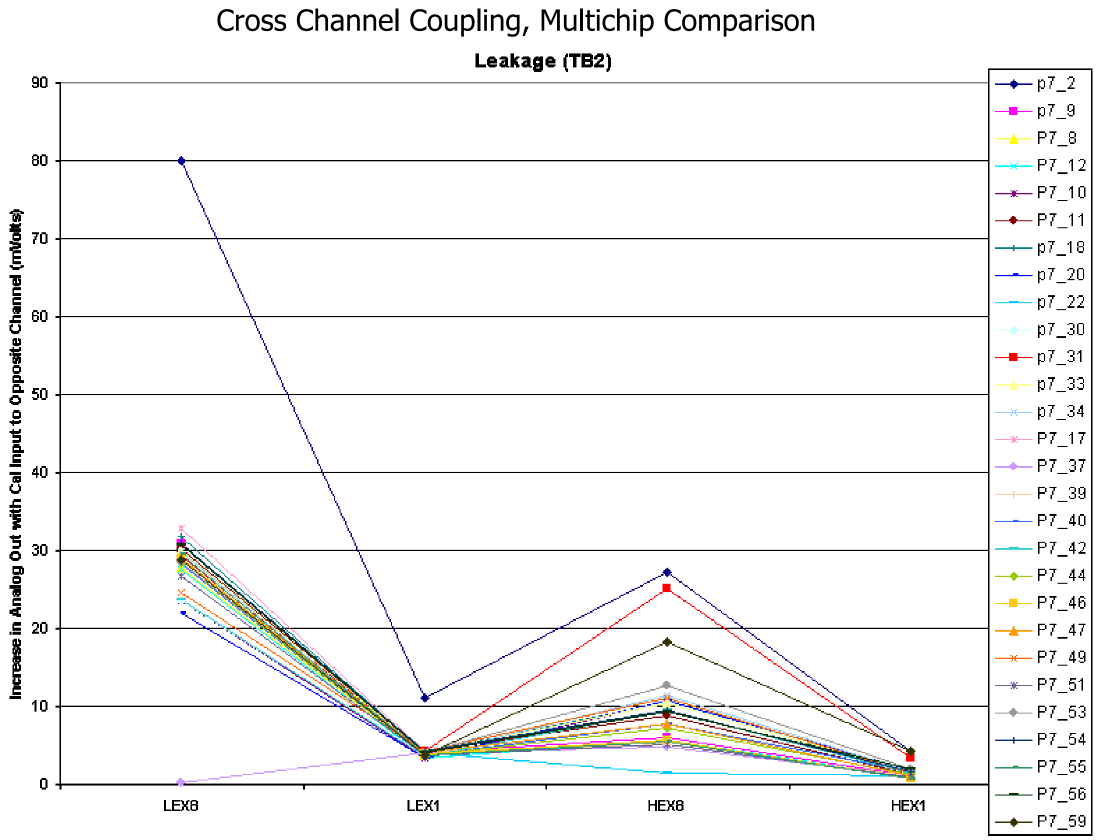
Cross Channel Coupling:

Cross channel coupling measurements were made by performing a calibration charge injection into one chip channel and looking for signal pickup in the other channel (ie. inject charge into low energy input only, look for signal at high energy output). Measurements showed a slight coupling effect.



Cross channel coupling was measured in 28 of the plastic package GCFE chips, for a fixed calibration input. This measurement was performed as a part of the functional test. Figure 32 shows that the coupling effects are generally the same in all but 2 of the 28 chips.

Figure 32 Compilation of cross channel coupling measurements for 28 GCFEs.



Power Consumption:

Power was measured with respect to the analog and digital supply inputs to the GCFE during the charge injection readout Aliveness test. A voltage measurement was taken with a Fluke 87 Multimeter across a 10 ohm series resistor for the analog supply, and across a 33 ohm resistor for the digital supply. For a population of seven chips, the typical analog supply current was measured to be 0.0145V/10 ohms = 1.45 mA and the digital supply current was measured to be 0.0575V/33 ohms = 1.7 mA. Operating from a 3.3V supply, the average power consumption is then 10.4 mWatts.

Thermal Testing:

Ten GCFE chips were thermally tested between 5° C and 45° C. An Omega Thermal-meter 5800 was used to monitor the temperature approximately 1.2" from the GCFE. Each chip was run under the Linear Noise Test with 16 data points. This process was repeated for 5° C, 22° C, 35° C and 45° C.

The temperature values are approximate, and intended to provide an estimate of chip performance over a temperature span. The hot environment was a closed cardboard box with injected heat, and the cold environment was a freezer.

The results of the Thermal Test show that the gain varies little with temperature. Though the gain of the x8 ranges does vary more than that of the x1 ranges. The graphs on the following pages show the gain for all energy ranges for the various temperatures with respect to GCFE p7_9. The results reflect the typical behavior of the thermally tested GCFE population.

Figure 33 Sample GCFE LEx8 gain variation over 40 Celcius temperature span.

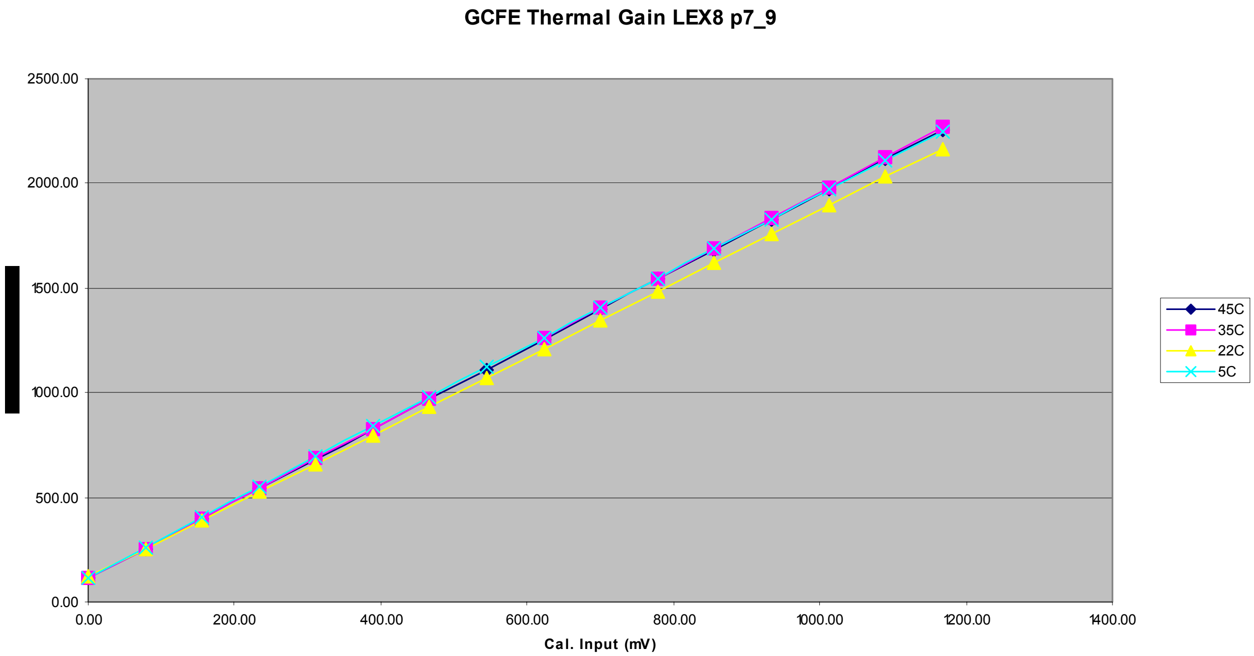


Figure 34 Sample GCFE LEx1 gain variation over 40 Celcius temperature span.

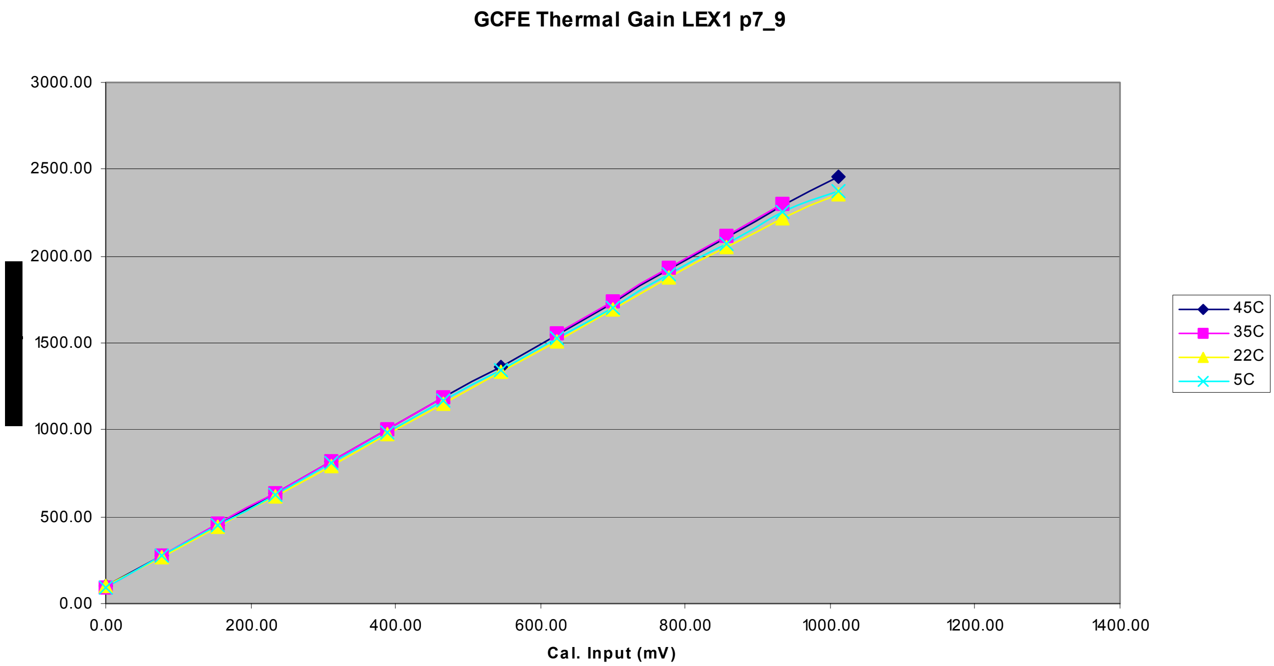


Figure 35 Sample GCFE HEx1 gain variation over 40 Celcius temperature span.

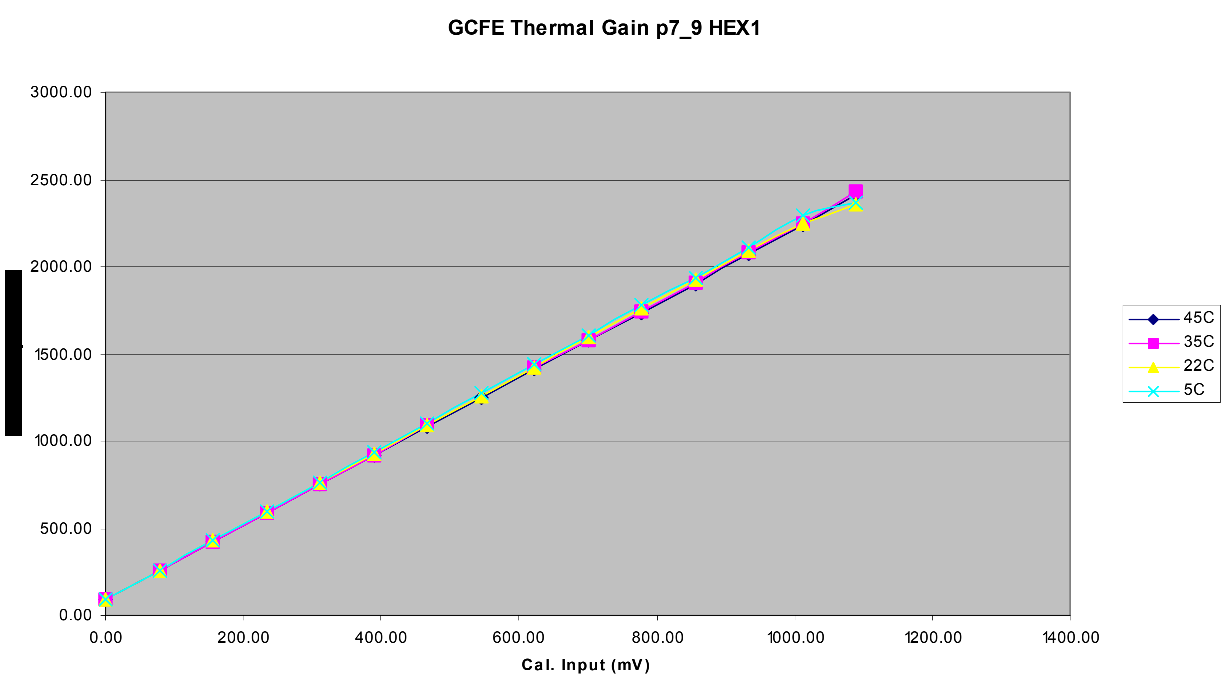
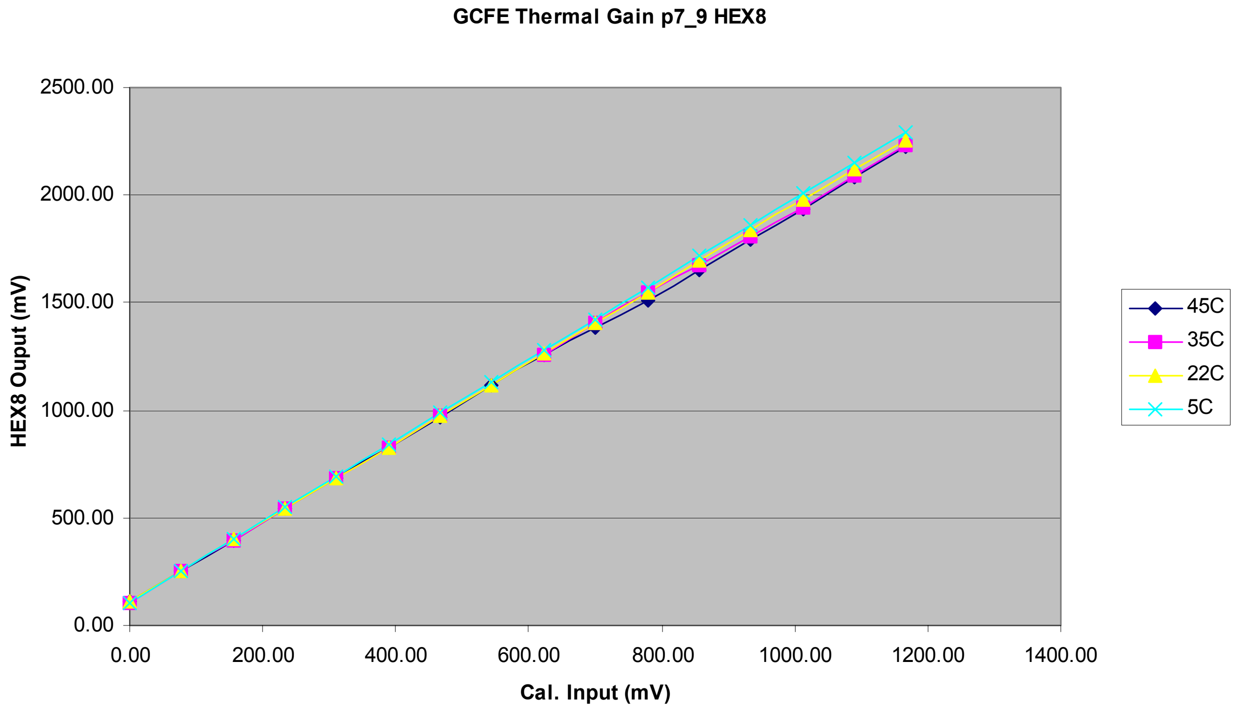


Figure 36 Sample GCFE HEx8 gain variation over 40 Celcius temperature span.



Appendix: Conversion from mV to MeV and e-:

The following describes the measurements made to calculate the conversions from mV to MeV or –e for the data above.

Step 1: Calibrate Shaper output
A pulse generator was used to inject a charge into the LE and HE input channels on the test board. For a fixed 5.0 pF series capacitor, the amplitude of the tail pulse and the slow shaper peaks were recorded over the effective range for each input. The results were plotted, verified to be linear, and the ratio of input to output calculated:

LE Slow Shaper Peak / Tail pulse peak = 8.9985
HE Slow Shaper Peak / Tail pulse peak = 0.8890

The series charge injection capacitance is 5 pF. The following is the conversion formula.

Injected Charge, Columbs = Capacitance, Farads * Tail pulse peak, volts

Injected Charge, electrons = Injected Charge, Coulombs / 1.6E-19 Columbs/electron

Equivalence to Energy deposited in CsI Log. The ratio is due to diode physical active area ratio. Actual conversion numbers may differ, but these are considered the GCFE design constants:

Low energy, 5,000 electrons per MeV
High Energy, 5,000 /6 electrons per MeV

Shaper output conversion from volts to input referred electrons, for x1 channels:

$$\text{e-/V (x1)} = \frac{\text{Injection Capacitance, Farads}}{\text{(1.6 E-19 C per e-) * (Shaper peak/Tail pulse peak Ratio)}}$$

Shaper output conversion from volts to input referred electrons, for x8 channels:
e-/V (x8) = e-/V (x1) / T&H Gain.
The Track & Hold x8 gain value is nominally 8. Exact value can be measured.

Shaper output conversion from volts to input referred MeV, for x1 channels:

$$\text{MeV/V (x1)} = \frac{\text{Injection Capacitance, Farads}}{\text{(e- per MeV) * (1.6 E-19 C per e-) * (Shaper peak/Tail pulse peak Ratio)}}$$

Shaper output conversion from volts to input referred MeV, for x8 channels:
MeV/V (x8 Chan) = MeV/V (x1) / T&H Gain
The Track & Hold x8 gain value is nominally 8. Exact value can be measured.

Step 2: Correlate Internal Calibration to Injected Charge
The internal calibration input that gives the equivalent slow shaper peak amplitude was determined for both HE and LE channels at both GCFE Calibration Gain 0 and 1 settings. From this comparison, the capacitance of the calibration signal was determined.

	Injected Tail Pulse Amplitude, V	Shaper Peak, V	External DAC Program Value	Measured Calibration Voltage, V	Computed Internal Calibration Capacitance, Farads
High Energy					
Gain = 0	0.251	0.221	xC40	0.953	1.32E-12
Gain = 1	0.351	0.31	x196	0.123	1.42E-11
Low Energy					
Gain = 0	0.0258	0.23	xCCC	0.996	1.30E-13
Gain = 1	0.0309	0.277	x184	0.1180	1.31E-12

Internal Calibration Capacitance computation:

$$\text{Cap, Farads} = \frac{\text{Ext. Charge Injection Capacitance (5.0 E-12 F) * Injected Tail Pulse Amplitude}}{\text{Measured Calibration Voltage}}$$

Step 3: Calculate Calibration Signal Conversions

The equation in Step 1 above are then used with the computed calibration capacitance values from Step 2, to calculate the conversion factors for using the calibration input source.

Results:

GCFE ASIC S/N 7.X		
Columbs/Electrons		1.60E-19
Electrons/MeV	LE	5000
	HE	800
Injected Pulse Capacitance		5.00E-12F

Injected Signal Conversion			**Calibration Signal Gain = 0**		**Gain = 1**	
	MeV / V	**e- / V**	**MeV / V**	**e- / V**	**MeV / V**	**e- / V**
LEX8	86.82	434,099	20.24	101,186	204.64	1,023,223
LEX1	694.56	3,472,792	161.90	809,486	1,637.16	8,185,785
HEX8	5,492.50	4,394,001	1,285.44	1,028,351	13,884.64	11,107,714
HEX1	43,940.01	35,152,004	10,283.51	8,226,806	111,077.14	88,861,710