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Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT) Calorimeter

Analog Front-End Electronics (AFEE) to Tower Electronics Module (TEM) – Interface Control Document

(Ver 1)

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Table of Contents

Table of Contents	4
List of Figures	5
List of Tables.....	5
1 Purpose.....	7
2 Scope	7
3 Definitions	7
3.1 Acronyms	7
4 Applicable Documents	7
5 Subsystem Overview.....	8
6 AFEE Coordinate System.....	11
7 Signal Interface	11
7.1 AFEE Board Connector.....	11
7.2 TEM to CAL signals	12
7.3 Signal Description	14
7.4 TEM to CAL Commanding Description	14
7.5 CAL Trigger Requests Description.....	21
7.6 RIGHT_FIRST Signal Description.....	21
7.7 Thermistor Connections	23
7.8 Commanding	24
7.9 Power	25

List of Figures

Figure 1: Calorimeter Exploded View.....	8
Figure 2 AFEE to TEM Layout.....	8
Figure 3: AFEE Board Block Schematic	10
Figure 4. AFEE/Calorimeter Log-end Numbering	11
Figure 5: 69-pin Contact Layout.....	11
Figure 6. AFEE Commanding and Data Return Signals	15
Figure 7. Command Signal Readout Timing.....	16
Figure 8. Generalized Log-End/ADC Data Return Order, per row. Right_First Not Asserted.....	16
Figure 9. Generalized Log-End/ADC Data Return Order, per row. Right_First Asserted.....	17
Figure 10. Interleaved Log-End/ADC Data Formatting per row, Single Range Readout, Right_First Not Asserted....	17
Figure 11. Interleaved Log-End/ADC Data Formatting per row, Single Range Readout, Right_First Asserted.....	18
Figure 12. Log-End/ADC Data Formatting per row, Four Range Readout Note that ranges 2 to 4 do not send log-accept bits.....	18
Figure 13. AFEE Command Load Definaton.....	19
Figure 14. Command Address Description.....	19
Figure 15. AFEE Command Read Timing fro m particular row.....	20
Figure 16. AFEE Command Read Timing from particular row.....	20
Figure 17. AFEE Trigger Requests to TEM	21
Figure 18. AFEE RIGHT_FIRST Usage.	22
Figure 19. AFEE RIGHT_FIRST Signal TEM Interface.....	22
Figure 20. AFEE Thermistor Signal TEM Interface.	23

List of Tables

Table 1 AFEE Connector Pin Assignment.....	13
Table 2 AFEE Signal Descriptions.....	14
Table 3. Readout (Trigger) Type Bit Definitions.....	16
Table 4. Minimum Successive Write Delays.....	20

Table 5. Read Response Delay Values	20
Table 6. RIGHT_FIRST Association per AFEE Side.....	22
Table 7. Command Function Bit Definitions	24
Table 8. GCRC Configuration Register Bit Definition.....	25
Table 9. GCRC Status Register Bit Definition.....	25

1 Purpose

The purpose of this document is to establish the electrical interface between the Calorimeter Analog Front-End Electronics (AFEE) and the Tower Electronics Module (TEM).

2 Scope

The scope of this document is the interface between the Calorimeter Front-End Electronics and the Tower Electronics Module. The interconnections are described below. The command/data formats and timing characteristics are defined in the LAT-SS-00208 Calorimeter Readout Control (GCRC) ASIC Conceptual Design Document.

3 Definitions

3.1 Acronyms

ADC – Analog to Digital Converter

AFEE – Analog Front-End Electronics (Circuit Board)

ASIC – Application-Specific Integrated Circuit

CAL – Calorimeter

COTS – Commercial Off-The-Shelf

DAC – Digital to Analog Converter

EMI – Electro-Magnetic Interference

GCFE – GLAST Calorimeter Front-End Electronics (ASIC)

GCRC – GLAST Calorimeter Readout Controller (ASIC)

GLAST – Gamma-ray Large Area Space Telescope

LAT – Large Area Telescope

PEM – Pre-Electronics Module

TBR – To Be Resolved

TEM – Tower Electronics Module

4 Applicable Documents

- LAT-TD-00242 Calorimeter Subsystem Preliminary Design Report
- LAT-SS-00278 Calorimeter Analog Front End Electronics (AFEE) Board Specification
- LAT-SS-00208 Calorimeter Readout Control (GCRC) ASIC Conceptual Design
- LAT-SS-00088 Calorimeter Front End (GCFE) ASIC Conceptual Design
- GSFC-433-RQMT GLAST EMI/EMC Requirements Document
- LAT Coordinate System, Version 1.2, Revised 6 November 2000 S. Ritz

5 Subsystem Overview

The calorimeter electronics consists of four electronics boards, called the analog front end electronics (AFEE), that are mounted on the sides of the PEM between the aluminum cell closeout and the outer EMI shield. See Figure 1.

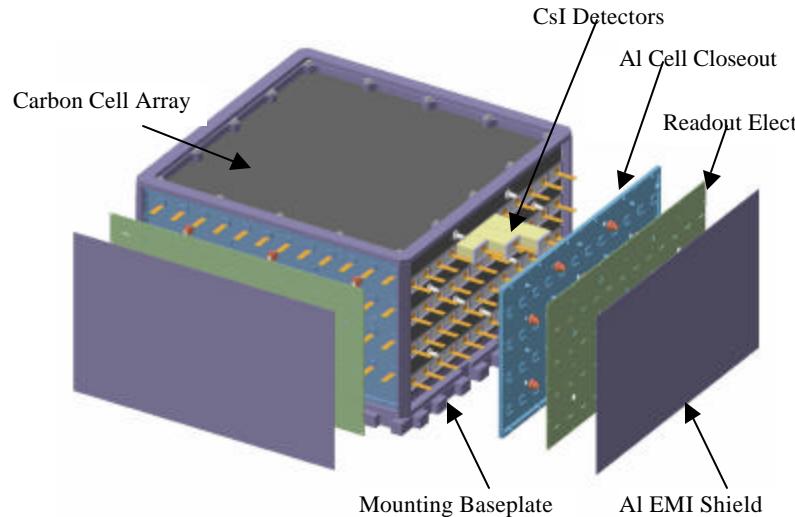


Figure 1: Calorimeter Exploded View

As shown in Figure 2 the four AFEE boards communicate with the Tower Electronics Module (TEM) that is mounted, along with the CAL power supply, underneath the PEM baseplate. The CAL controller, which is part of the TEM, merges the data from the four AFEE cards into a CAL event packet which is combined with Tracker and Trigger system data for transmission to the Trigger and Data Flow system for analysis.

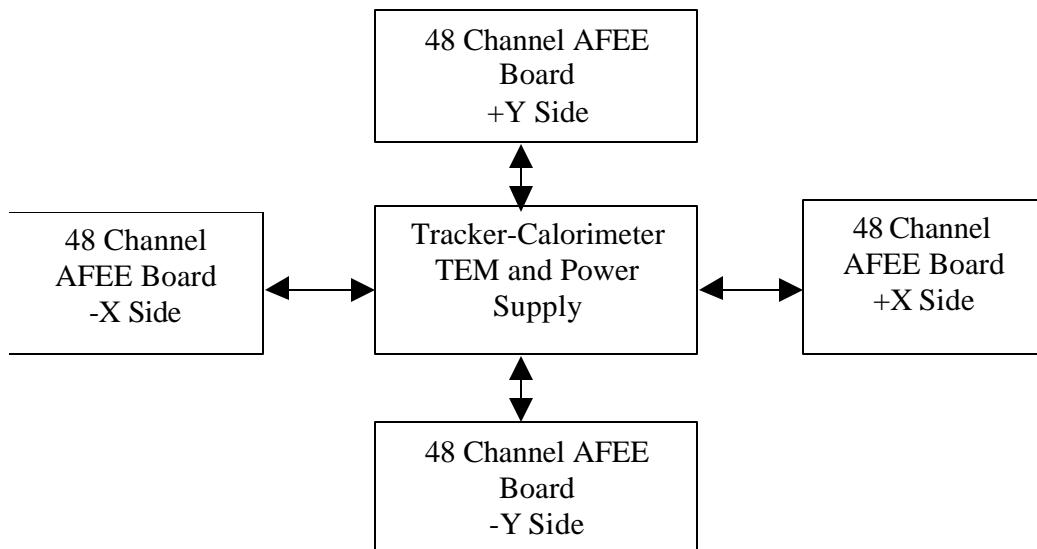
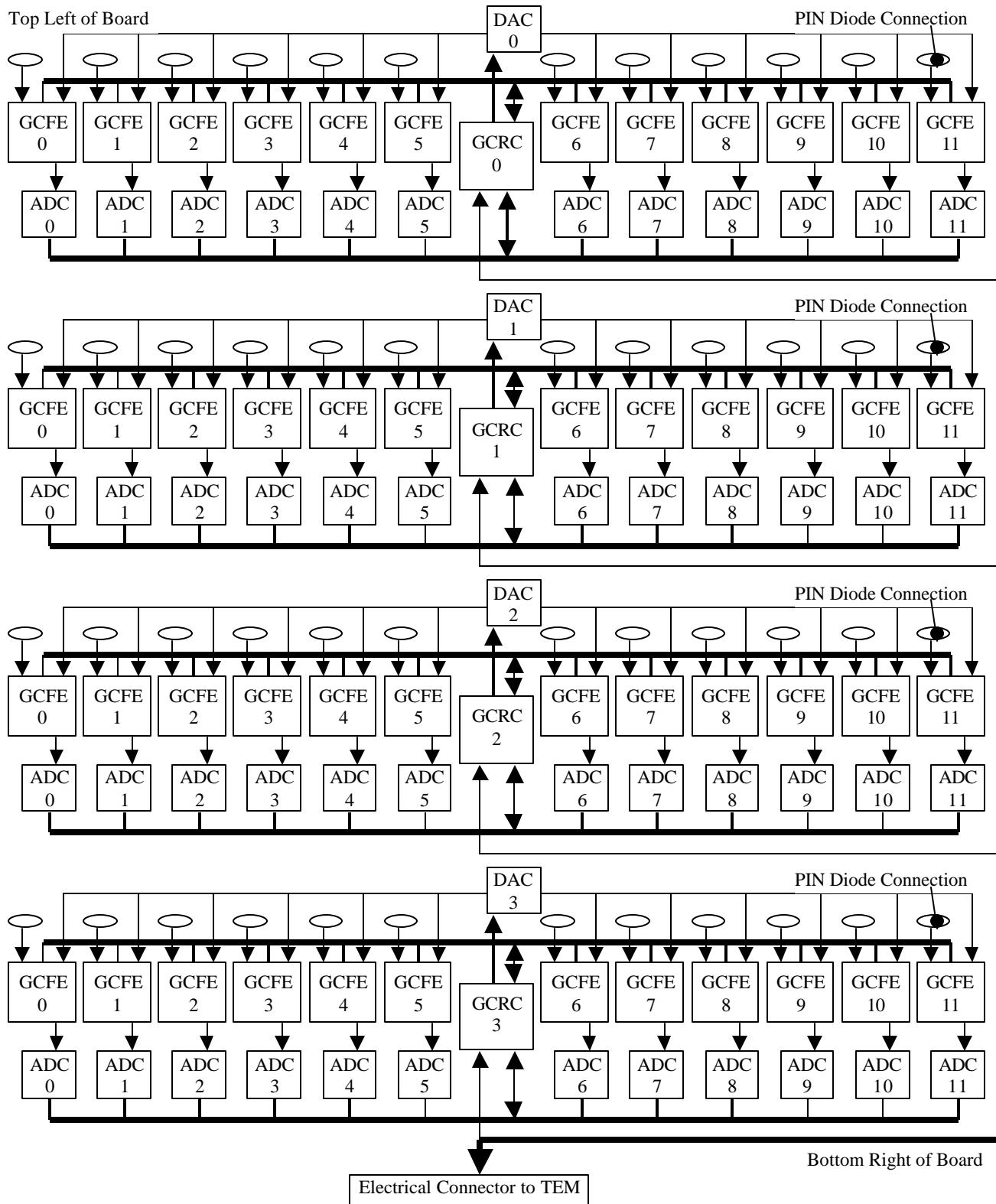


Figure 2 AFEE to TEM Layout.

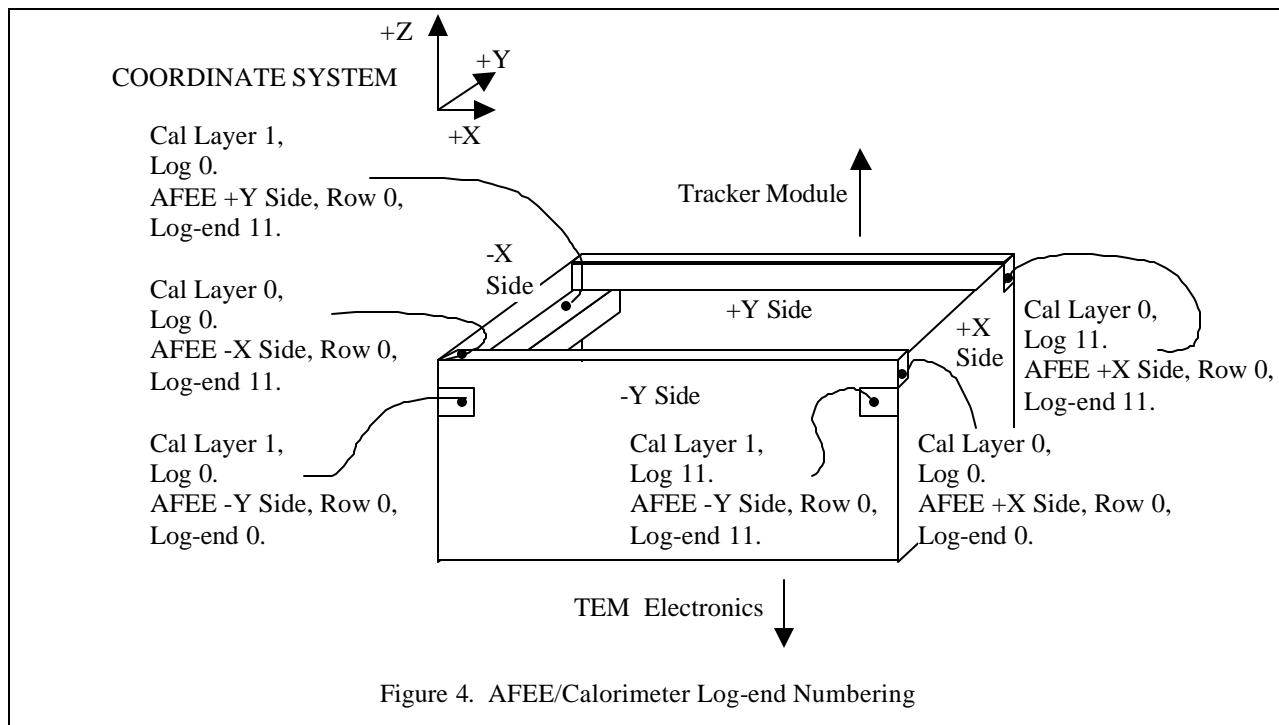
Each of the four AFEE boards serves one side of the calorimeter. The calorimeter side is comprised of 48 crystal ends, organized in 4-layers of 12. Figure 3 shows a schematic AFEE board.

The board description is started at the signal source, the off-board PIN diodes, residing below the AFEE board. A connection from each PIN diode is made through a slot in the board to a dedicated GLAST Calorimeter Front-End (GCFE) ASIC's by means of a flexible Kapton cable. The processed analog signal from each GCFE is then digitized by a dedicated Analog to Digital Converter (ADC). Each of the four GLAST Calorimeter Readout Controller (GCRC) ASICs then combines bits from each of their 12 ADCs per layer with information from their respective layer GCFE chips and transmits the data packet to the TEM. The GCRC chips can additionally handle register read/writes from the Tower electronics Module (TEM) to a particular GCFE or GCRC device. The TEM commands the described readout process, being initiated from trigger requests originating from GCFEs transmitted through the GCRC chips, or from other sub-system trigger requests.

Better defining the signal connections, each layer of the AFEE is independently controlled by a single GLAST Calorimeter Readout Controller (GCRC). A single GCRC controls 12 GLAST Calorimeter Front-End (GCFE) ASIC's. A parallel bus performs commanding to the GCFEs, but data readback is performed individually from each GCFE. 12 Analog to Digital Converters (ADCs) are likewise commanded in parallel, but serial data read is read back on individual lines. The serial Digital to Analog Converter (DAC), used for calibration of the GCFEs, is separately addressed. Each GCRC transmits data to the TEM on two data lines, resulting in shorter transmit time. There is one connector to the TEM for both signaling and power. The AFEE board contains a total of 48 GCFE chips, 4 GCRC chips, 48 commercial ADCs, 4 commercial DACs, 48 PIN diode connections, electrical connector, resistors and capacitors.

Figure 3: AFEE Board Block Schematic

6 AFEE Coordinate System



The local coordinate system for a Calorimeter module follows the GLAST LAT coordinate system. The layer numbering starts at the top of the Calorimeter, Layer 0, the side nearest the Tracker. The layer numbering increments in the direction towards the TEM electronics (downwards in **Figure 4**), ending at layer 7 nearest the TEM electronics. The crystal log numbering per layer is referenced with the zero numbered log to the left when looking at the +X or +Y side. The layer log numbering increments to the right, again when looking at the +X or +Y side. Since each side of the calorimeter sides only interfaces with four crystal layers, “row” is used for vertical referencing of the AFEE boards. Thus both the X and Y sides have four rows, row 0 being closest to the Tracker, and row 4 being closest to the TEM electronics. For horizontal log-end positioning on the AFEE boards, log-end 0 is always to the left when facing the front of the AFEE board.

7 Signal Interface

7.1 AFEE Board Connector

Each AFEE board contains interfaces to the TEM through a single connector. The connector is a right angle 69-pin micro-D Receptacle, M83513 type, manufactured by Cristek Interconnects, Inc. or Airborn, Inc. The Cristek part number is MCR-1069-2B1. The pin arrangement is illustrated in Figure 5.

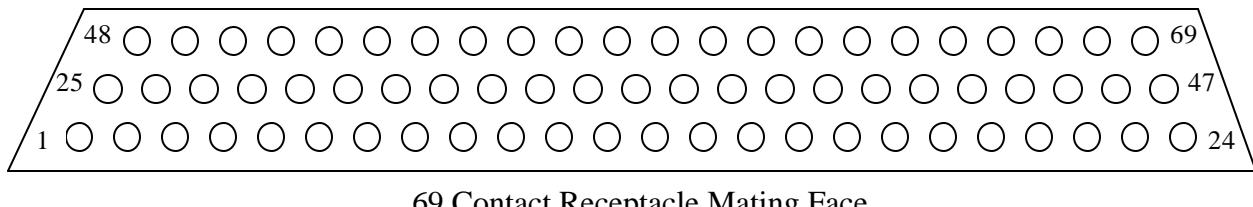


Figure 5: 69-pin Contact Layout

Pins on the left and right edges of the connector are unused by the calorimeter. Space in the connector body for the outer pins is reserved for possible helicoil inserts into the plastic body. The helicoils are threaded inserts for mechanical fastening of the connector to the AFEE board. The TEM grounds the connector pins unused by the AFEE.

7.2 TEM to CAL signals

Note that in signal naming, signals between the TEM and GCRC begin with the letters “CAL_” indicating Calorimeter subsystem. Additionally, signals that are asserted low, have a “N” prefix in the root name. For example the signal name “CAL_NCMD” indicates it is a Command line (CMD) between the Calorimeter and TEM, asserted low. Output signals for which there is one per AFEE row have a suffix number indicating row. Lastly, differential signals have a suffix of either “P” denoting positive zero level or suffix “M” denoting minus zero level. For example, signal CAL_NTREQLE1P is a Calorimeter subsystem signal asserted low, from layer 1 and is differential positive.

Also note that unused pins are to be grounded to the TEM ground. The AFEE side of these connections will be floating.

Table 1 AFEE Connector Pin Assignment.

Number	Signal	AFEE In/Out	Number	Signal	AFEE In/Out
1	Unused, TEM Gnd	N/A	36	CAL_NDATA1_3P	Output
2	CAL_NRESETP	Input	37	CAL_NDATA1_3M	Output
3	CAL_NRESETM	Input	38	CAL_NTREQLE4P	Output
4	CAL_NCMDP	Input	39	CAL_NTREQLE4M	Output
5	CAL_NCMDM	Input	40	CAL_NTREQHE4P	Output
6	CAL_CLKP	Input	41	CAL_NTREQHE4M	Output
7	CAL_CLKM	Input	42	CAL_NDATA0_4P	Output
8	CAL_NTREQLE1P	Output	43	CAL_NDATA0_4M	Output
9	CAL_NTREQLE1M	Output	44	CAL_NDATA1_4P	Output
10	CAL_NTREQHE1P	Output	45	CAL_NDATA1_4M	Output
11	CAL_NTREQHE1M	Output	46	Unused, TEM Gnd	N/A
12	CAL_NDATA0_1P	Output	47	Unused, TEM Gnd	N/A
13	CAL_NDATA0_1M	Output	48	Unused, TEM Gnd	N/A
14	CAL_NDATA1_1P	Output	49	Unused, TEM Gnd	N/A
15	CAL_NDATA1_1M	Output	50	CAL_RIGHT_FIRST	Input
16	CAL_NTREQLE2P	Output	51	CAL_RIGHT_RET	Power
17	CAL_NTREQLE2M	Output	52	3.3V ANALOG	Power
18	CAL_NTREQHE2P	Output	53	3.3V ANALOG	Power
19	CAL_NTREQHE2M	Output	54	ANA RET	Power
20	CAL_NDATA0_2P	Output	55	ANA RET	Power
21	CAL_NDATA0_2M	Output	56	CAL_THERMOP	Output
22	Spare	N/A	57	CAL_THERMOM	Output
23	Unused, TEM Gnd	N/A	58	3.3V DIGITAL	Power
24	Unused, TEM Gnd	N/A	59	3.3V DIGITAL	Power
25	Unused, TEM Gnd	N/A	60	DIG RET	Power
26	Unused, TEM Gnd	N/A	61	DIG RET	Power
27	Unused, TEM Gnd	N/A	62	CAL_THERM1P	Output
28	CAL_NDATA1_2P	Output	63	CAL_THERM1M	Output
29	CAL_NDATA1_2M	Output	64	BIAS RET	Power
30	CAL_NTREQLE3P	Output	65	BIAS RET	Power
31	CAL_NTREQLE3M	Output	66	BIAS VOLTAGE	Power
32	CAL_NTREQHE3P	Output	67	BIAS VOLTAGE	Power
33	CAL_NTREQHE3M	Output	68	Unused, TEM Gnd	N/A
34	CAL_NDATA0_3P	Output	69	Unused, TEM Gnd	N/A
35	CAL_NDATA0_3M	Output			

7.3 Signal Description

Table 2 AFEE Signal Descriptions.

CAL_NRESET	Reset command from TEM. Bussed to all 4 GCRCs.
CAL_CLK	System Clock from TEM (20 MHz). Bussed to all 4 GCRCs.
CAL_NCMD	Command from TEM. Bussed to all 4 GCRCs.
CAL_NTREQLE0	L1 Low Energy Trigger Request, Cal row 0, to TEM.
CAL_NTREQLE1	L1 Low Energy Trigger Request, Cal row 1, to TEM.
CAL_NTREQLE2	L1 Low Energy Trigger Request, Cal row 2, to TEM.
CAL_NTREQLE3	L1 Low Energy Trigger Request, Cal row 3, to TEM.
CAL_NTREQHE0	L1 High Energy Trigger Request, Cal row 0, Request to TEM.
CAL_NTREQHE1	L1 High Energy Trigger Request, Cal row 0, Request to TEM.
CAL_NTREQHE2	L1 High Energy Trigger Request, Cal row 0, Request to TEM.
CAL_NTREQHE3	L1 High Energy Trigger Request, Cal row 0, Request to TEM.
CAL_NDATA0_0	Data to TEM, "Pipe" 0 of Cal row 0.
CAL_NDATA1_0	Data to TEM, "Pipe" 1 of Cal row 0.
CAL_NDATA0_1	Data to TEM, "Pipe" 0 of Cal row 1.
CAL_NDATA1_1	Data to TEM, "Pipe" 1 of Cal row 1.
CAL_NDATA0_2	Data to TEM, "Pipe" 0 of Cal row 2.
CAL_NDATA1_2	Data to TEM, "Pipe" 1 of Cal row 2.
CAL_NDATA0_3	Data to TEM, "Pipe" 0 of Cal row 3.
CAL_NDATA1_3	Data to TEM, "Pipe" 1 of Cal row 3.
CAL_RIGHT_FIRST	Control Bit, Swaps log-end left/right readout order when asserted high. Asserted by TEM.
CAL_RIGHT_FIRST_RET	Return for Right First control .
CAL_THERM0P	Analog connection to thermistor 0 for sensing AFEE board temperature.
CAL_THERM0M	Return for thermistor 0.
CAL_THERM1P	Analog connection to thermistor 1 for sensing AFEE board temperature.
CAL_THERM0M	Return for thermistor 1.
3.3V ANALOG	Analog Supply, nominally 3.3 Volts
ANA RET	Return for Analog Supply
3.3V DIGITAL	Digital Supply, nominally 3.3 Volts
DIG RET	Return for Digital Supply
BIAS VOLTAGE	High Voltage (70-100 Volt) Supply for PIN Photodiode bias.
BIAS RET	Return for Bias Voltage Supply

7.4 TEM to CAL Commanding Description

The TEM to AFEE commanding uses a two wire interface consisting of a constant 20 MHz system clock, CAL_CLK, and command line, CAL_NCMD. Command replies back to the TEM from an AFEE consist of 8 data lines, with root name CAL_NDATA. The 8 return data lines are clocked synchronous to the 20 MHz system clock and are partitioned as two data lines per AFEE row. A reset line to the calorimeter, CAL_NRESET, forces the calorimeter controller to a known zero state. All of the commanding signals are differential LVDS format, with the CAL_NCMD, CAL_NRESET, and CAL_NDATA lines asserted low.

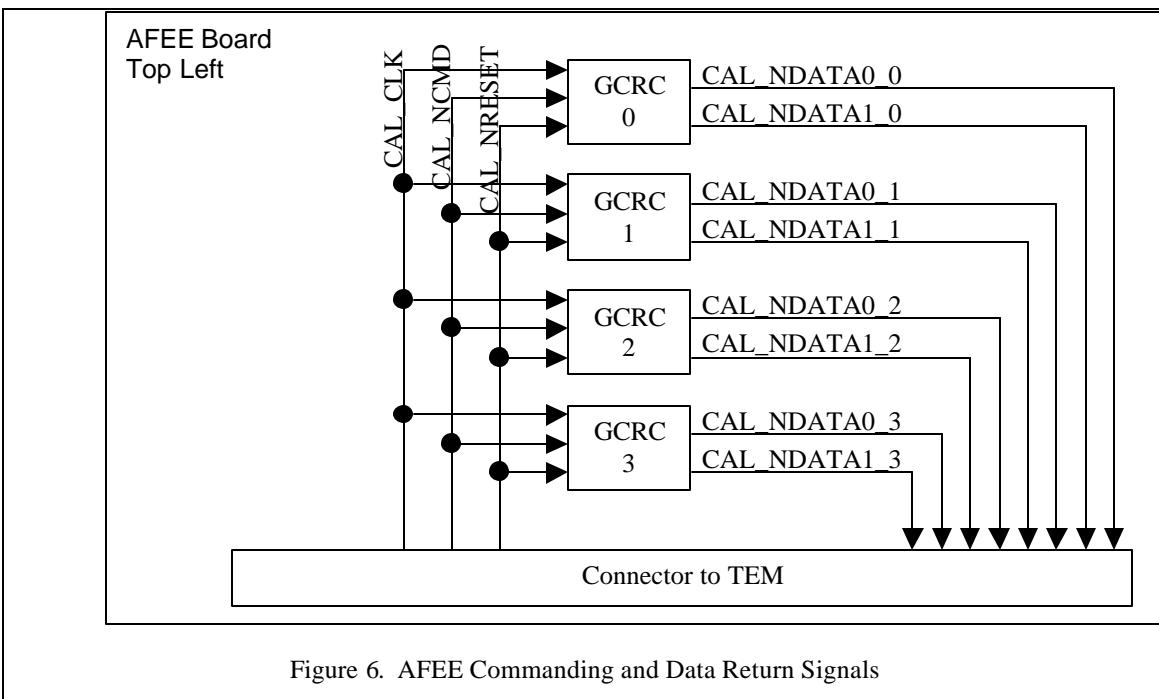


Figure 6. AFEE Commanding and Data Return Signals

The TEM command is one of three types:

- Command Signal Readout (Trigger), used for reading out the crystal end analog data.
- Command Register Load, used for configuring the GCRC and GCFE devices. Through address bits in the TEM command, the load command can address a particular GCFE or GCRC, whole row of GCFEs, whole column of GCFEs, or whole AFEE board.
- Command Register Read. The read commands are used for verifying the GCRC and GCFE registers, and for getting returned status information.

Signal Readout:

The nominal readout operation is digitization of one of the four possible GCFE ranges per log end. The trigger command from the TEM can specify readout of one or all four GCFE ranges (Figure 3 and Table 3). For single range readout, the GCFE chips are nominally allowed to decide their own optimum range to readout per event, based upon crystal-end signal level. Thus for correct association of the ADC data, AFEE sends two range definition data bits per range digitized. The range definition bits are passed with the ADC data to the TEM.

Zero suppression, the process of discarding minimal amplitude data, is made easier with a dedicated discriminator bit in each GCFE chip. The log-accept bit is again passed with the ADC data, enabling the TEM to quickly zero suppress data with no computation.

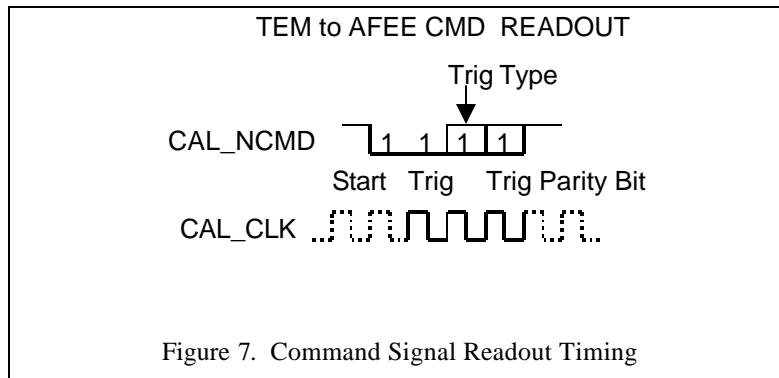
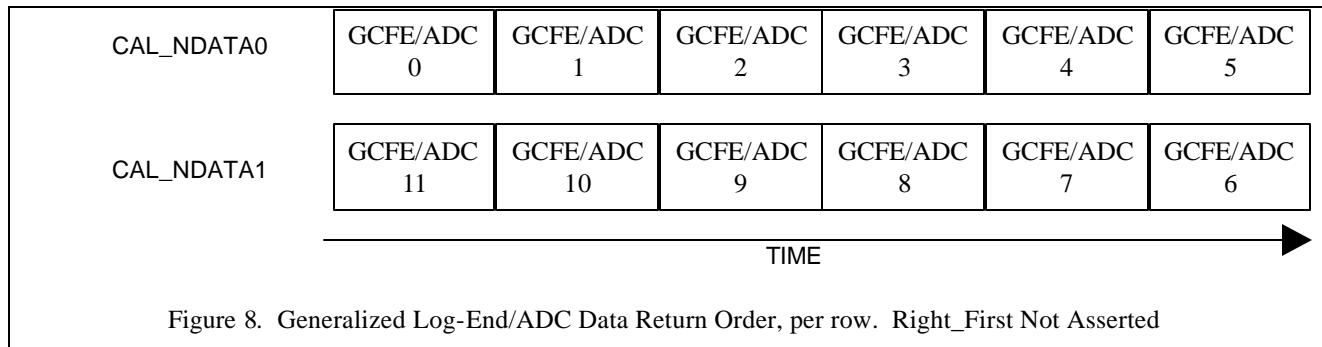


Table 3. Readout (Trigger) Type Bit Definitions

Bit Value	Definition
0 high	1 Readout Range
1 Asserted Low	4 Range Readout

Figure 7 shows signal command for range readout operation. **Table 3** defines the bits for requesting 1 or 4 range readout.

The data returned by the AFEE from the readout command follows a preset order so that the TEM can associate data with log-ends. The AFEE always transmits all the log-end information. **Figure 8** Shows the general log-end readout order per AFEE row, for sides with the RIGHT_FIRST not asserted, +X and +Y sides. **Figure 9** shows the general log-end readout order per AFEE row for the RIGHT_FIRST asserted sides, -X and -Y sides. **Figure 10** shows the interleaving of the readout data bits per AFEE row, in transmission to the TEM, for the non RIGHT_FIRST asserted sides. **Figure 11** shows the interleaving of the readout data bits per AFEE row, in transmission to the TEM, for the RIGHT_FIRST asserted sides. **Figure 12** shows the data packet organization for 4 range readout, which has four separate data packets transmitted to the TEM, of two different bit lengths.



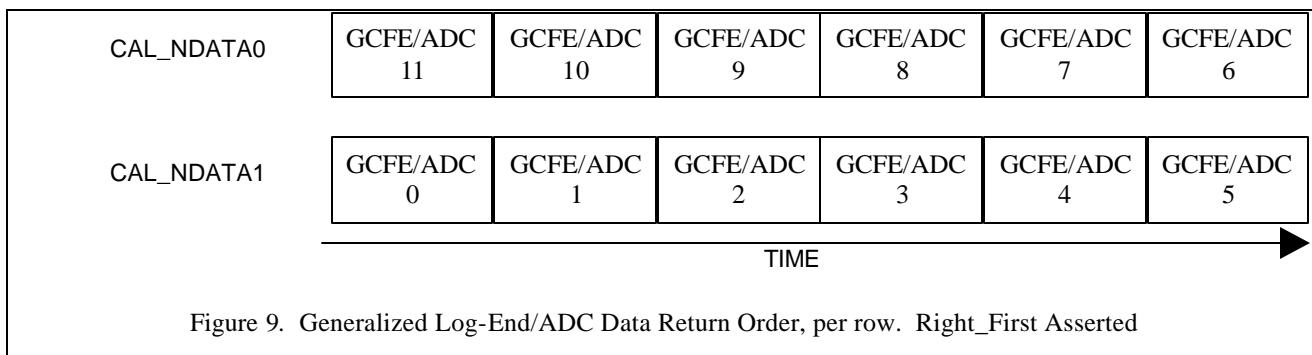


Figure 9. Generalized Log-End/ADC Data Return Order, per row. Right_First Asserted

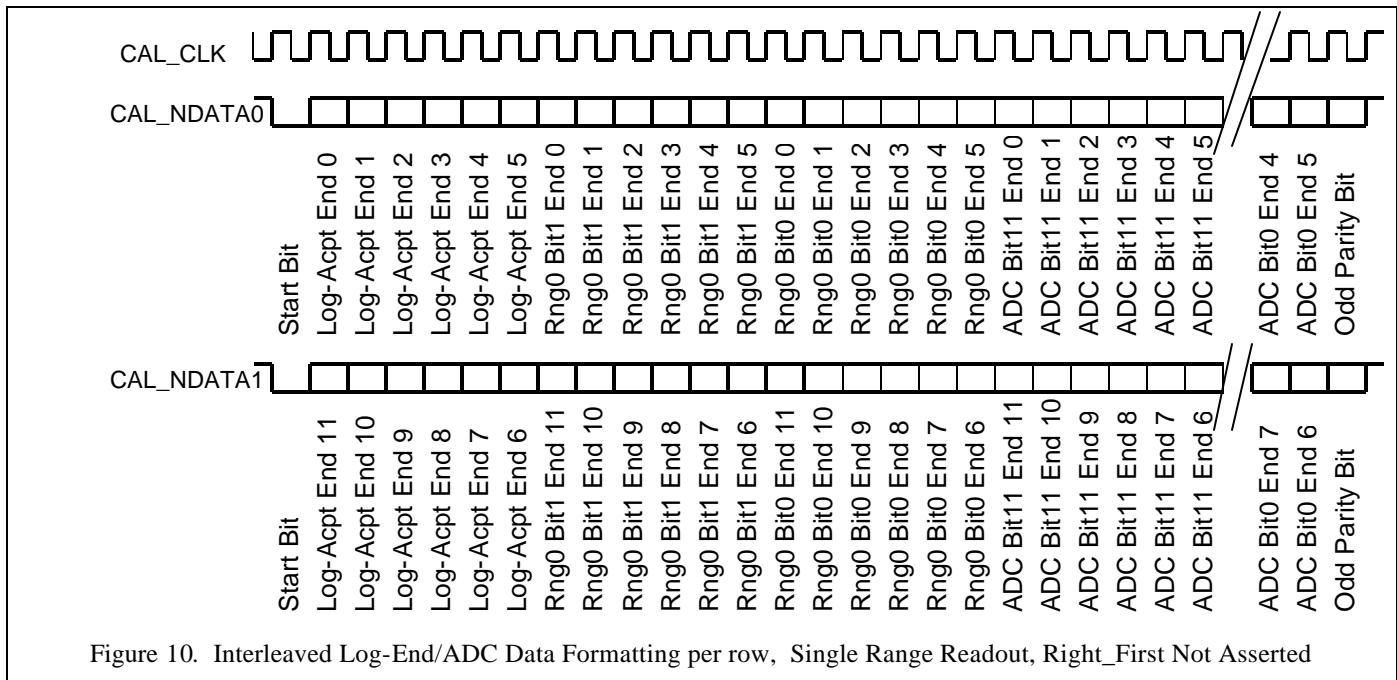
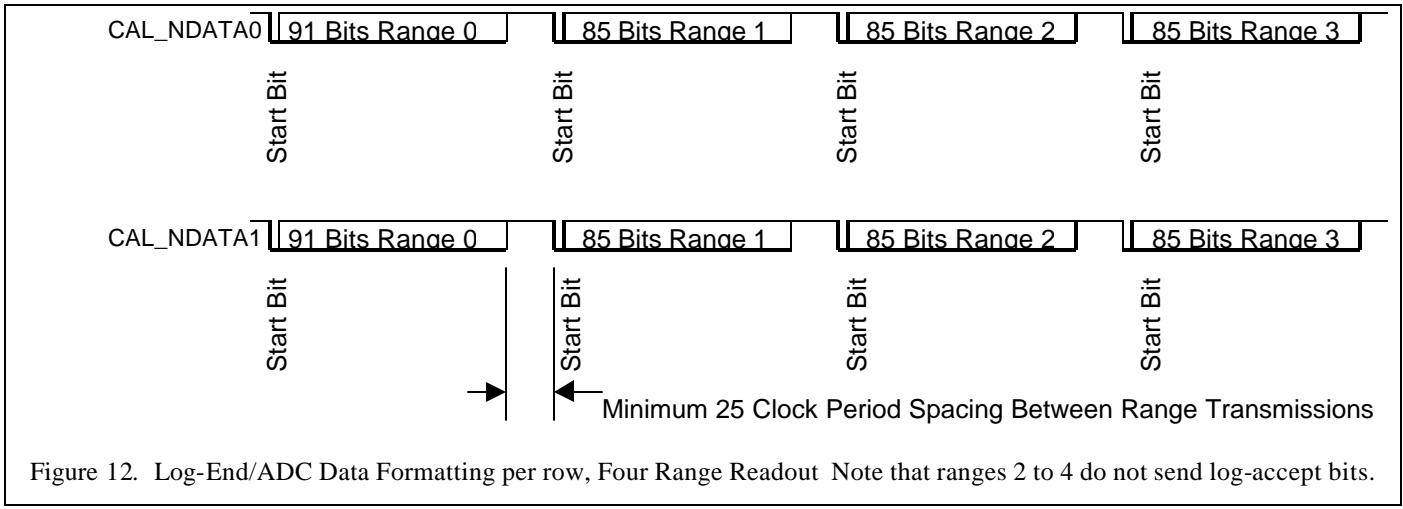
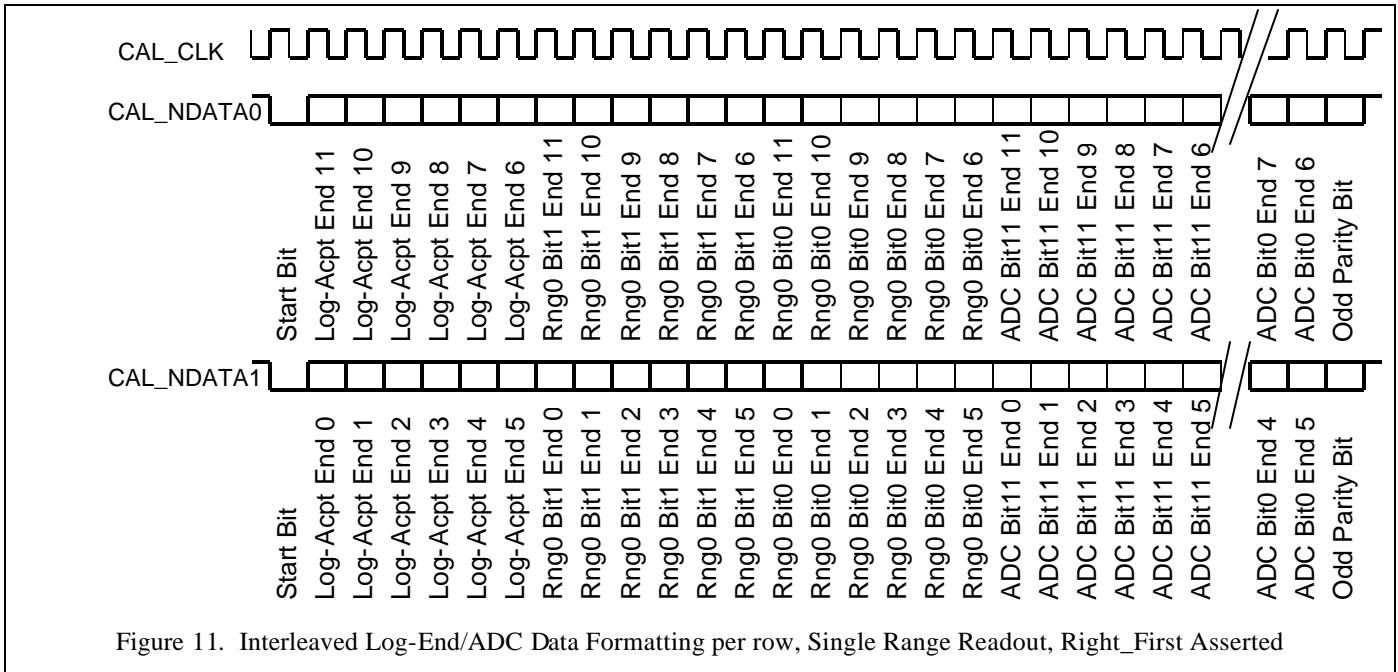
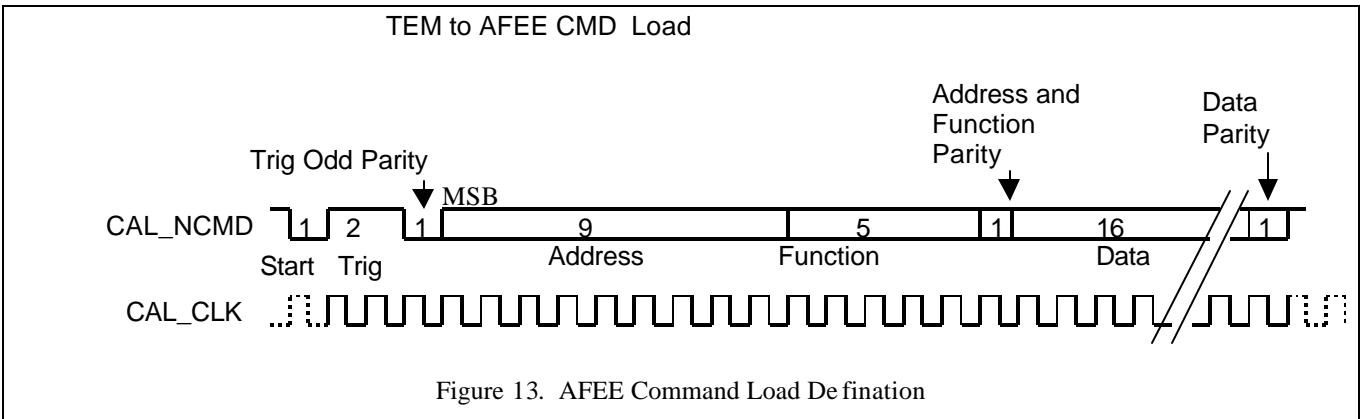


Figure 10. Interleaved Log-End/ADC Data Formatting per row, Single Range Readout, Right_First Not Asserted

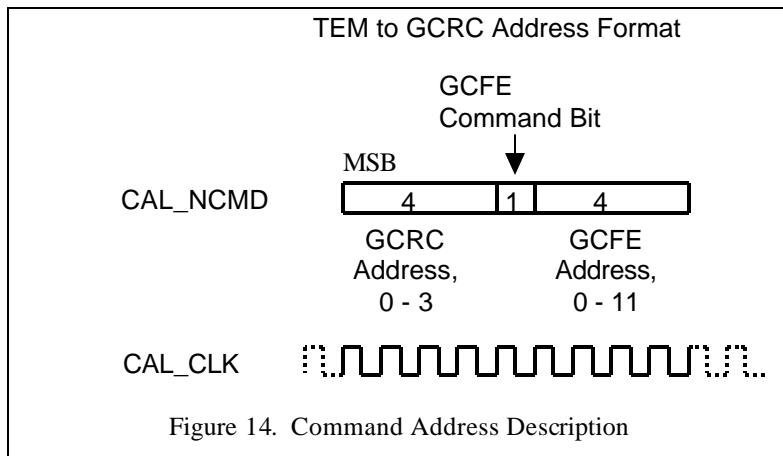


Command Register Load:

The TEM to AFEE register load structure is defined in **Figure 13**. Following the trigger bits which define no trigger, a 9 bit address is transmitted, then a five bit function code (refer to **Table 7**), followed by an address and function parity bit (refer to **Table 8**) followed by a 16 bit data field, followed by the data field parity bit.



The address bits are further defined in **Figure 14** showing that the GCRC 4 bit address is transmitted first, followed by a single GCFE command bit which is asserted true for a command directed to the GCFEs, and lastly the 4 bit GCFE address. The two most significant bits of the GCRC address are not actually used in that only two bits are required to define the four row selection per AFEE.



The AFEE hardware has a limit on how closely spaced in time it can handle successive commands. **Figure 15** shows that the definition in spacing that will be used is the time between the last bit transmitted from the first command and the time in which the start bit is transmitted in the second command. The minimum successive delays are defined in **Table 4**. It is expected that for GCRC version greater than 1, the minimum time for successive GCFE writes will be reduced to the same 3 clock cycles as for the other commands.

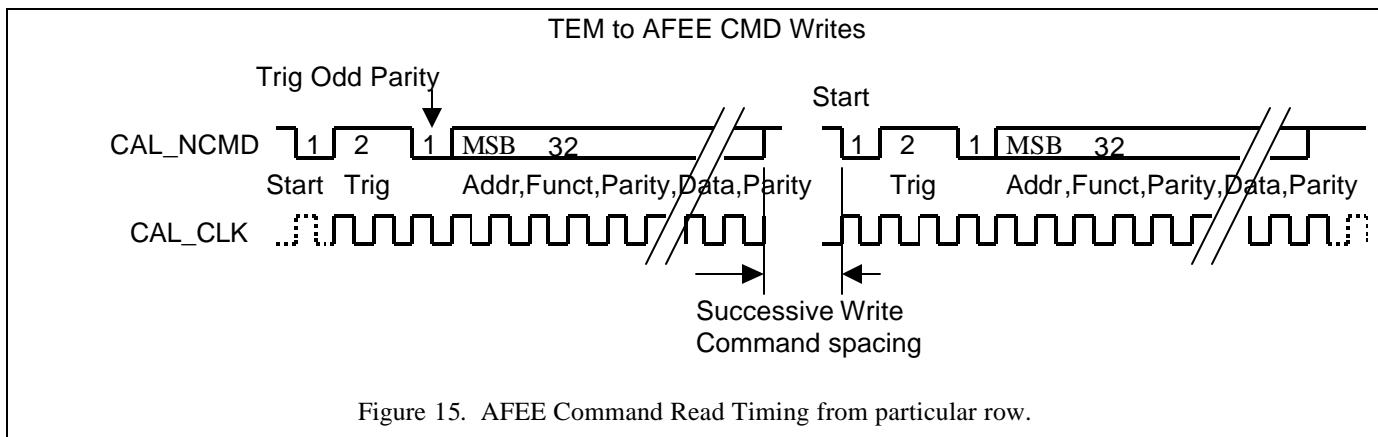


Table 4. Minimum Successive Write Delays

First Action	Second Action	Minimum Delay
GCRC Write	GCRC Read/Write, GCFE Read/Write or Readout	3 Clk Cycles
GCFE Write	GCRC Read/Write, GCFE Read/Write or Readout	15 Clk Cycles (GCRC Ver. 1)
DAC Write	GCRC Read/Write, GCFE Read/Write or Readout	3 Clk Cycles
DAC Write	DAC Write	33 Clk Cycles

Figure 16 shows the command structure and response delay definition for AFEE read commands. The command structure is similar to the load commands, but shorter without a required data field or data parity. The command reply repeats the address and function bits, adds parity according to the particular GCRC configuration register, follows with 16 bits of data , status error flag, and then data-status error parity. The maximum and minimum read response delay values are shown in **Table 5**.

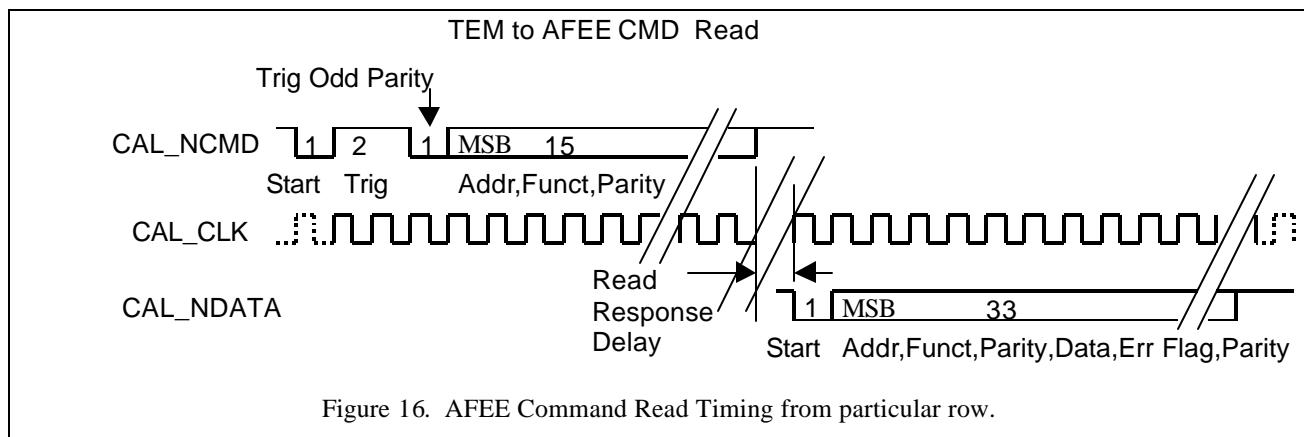


Table 5. Read Response Delay Values

Action	Min Delay	Max Delay
GCRC Read	3 Clk Cycles	3 Clk Cycles
GCFE Read	15 Clk Cycles	40 Clk Cycles (GCFE Response Timeout)
DAC Read	3 Clk Cycles	3 Clk Cycles

7.5 CAL Trigger Requests Description

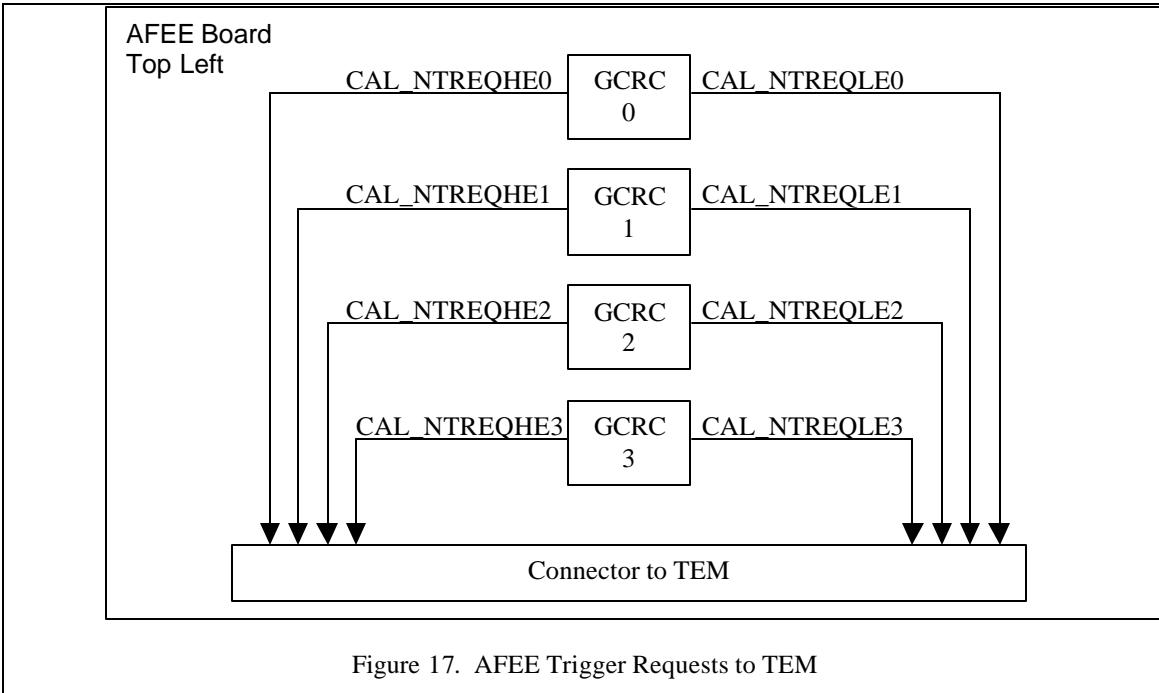


Figure 17. AFEE Trigger Requests to TEM

Trigger requests to the TEM are on the CAL_NTREQHE and CAL_NTREQLE lines, as shown in **Figure 17**. The signaling format is minimum pulse width of 200 nsec, and maximum pulse length is time-over-threshold. The trigger communication lines between the GCRC and TEM are LVDS, asserted low.

7.6 RIGHT_FIRST Signal Description.

The Calorimeter RIGHT_FIRST signal is used to switch the left – right association on the AFEE board, so that two opposing AFEE board's (ie. X+ and X-) log-ends are logically addressed the same. The RIGHT_FIRST addressing is used both in register read/writes and range readout. **Figure 18** shows that with opposing AFEEs having opposite RIGHT_FIRST assertions, an addressed command will be directed to the same log electronics. In a similar manner, for range readout, the data bits from both ends of the same crystal log will arrive at the TEM at the same time. **Table 6** defines how the TEM will assert the RIGHT_FIRST signal for all 4 Calorimeter sides. To minimize noise coupling between the TEM and AFEE, a special filter circuit is defined in **Figure 19**. The RIGHT_FIRST signal is treated as a DC level that will not change, and can therefore have large resistor-capacitor filtering.

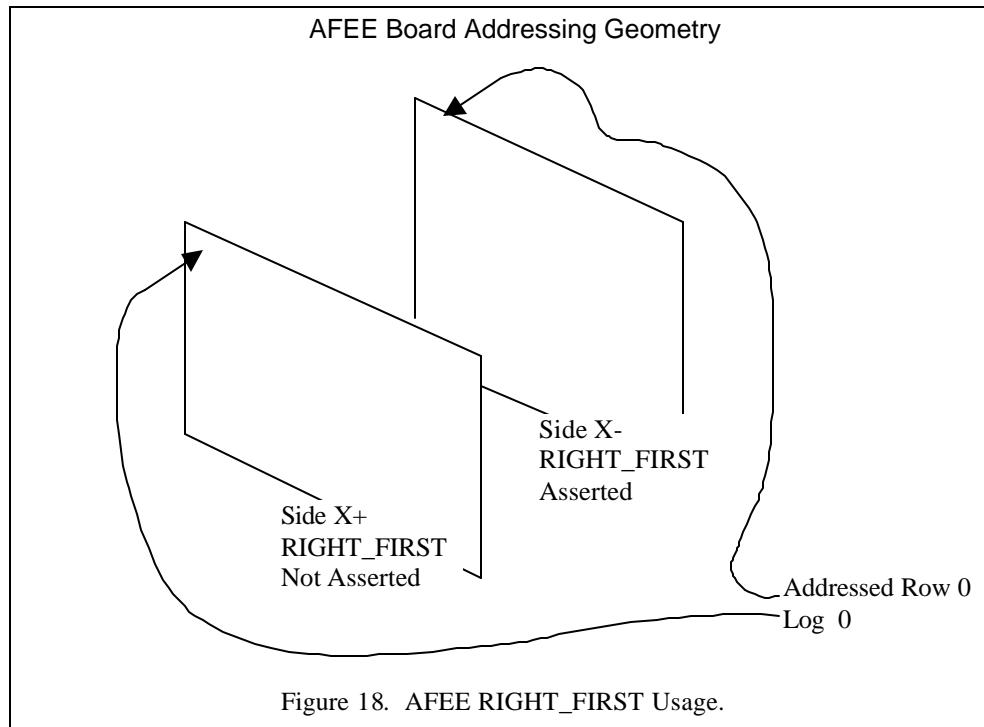
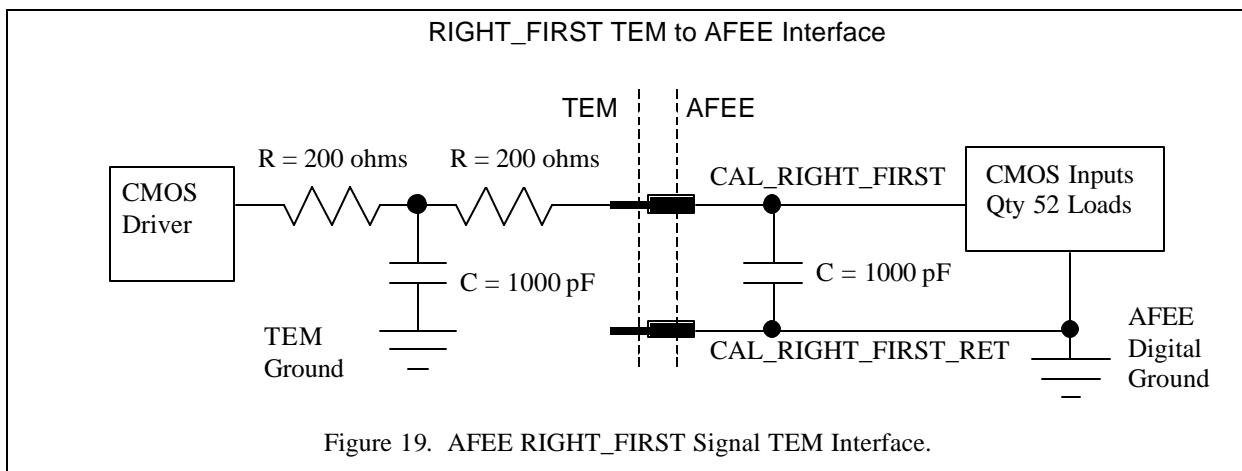


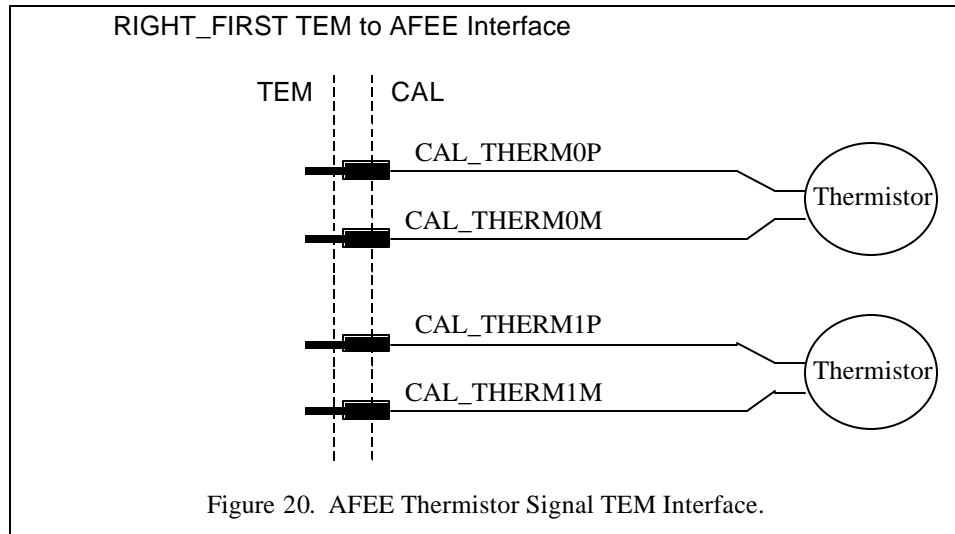
Table 6. RIGHT_FIRST Association per AFEE Side

AFEE Side	Assertion Level of RIGHT_FIRST
+X	Low
+Y	High, switch left - right addressing.
-X	High, switch left - right addressing.
-Y	Low



7.7 Thermistor Connections

The AFEE has connections for two thermistors for spacecraft temperature monitoring whether the AFEE is powered or not. The AFEE passes the thermistor signals directly to the TEM. The thermistor placement is **TBD**.



7.8 Commanding

Table 7. Command Function Bit Definitions

GCFE Ver 1-4, Function Bits	GCFE Ver >= 5, Function Bits	Definition	Data Bits 15-8 Write Key	Number of Effective Data Bits
00000	00000	Write not used		
00001	00001	Write Reset GCRC		
00011	00011	Calibration strobe to GCFEs command		
00100	01000	<i>Write GCFE Config Reg 0</i>		13 bits
10100	10000	<i>Read GCFE Config Reg 0</i>		
00101	01001	<i>Write GCFE Config Reg 1</i>		7 bits
10101	10001	<i>Read GCFE Config Reg 1</i>		
00110	01010	<i>Write GCFE Fast Low Energy DAC</i>		7 bits
10110	10010	<i>Read GCFE Fast Low Energy DAC</i>		
00111	01011	<i>Write GCFE Fast High Energy DAC</i>		7 bits
10111	10011	<i>Read GCFE Fast High Energy DAC</i>		
01000	01100	<i>Write GCFE Log Accept DAC</i>		7 bits
11000	10100	<i>Read GCFE Log Accept DAC</i>		
01001	01101	<i>Write GCFE Upper Level Discrim DAC</i>		7 bits
11001	10101	<i>Read GCFE Upper Level Discrim DAC</i>		
01010	01110	<i>Write GCFE Reference DAC</i>		7 bits
11010	10110	<i>Read GCFE Reference DAC</i>		
01011	01011	Write Time Delay 1, Peak Hold to GCFE Range decision		6 bits
11011	11011	Read Time Delay 1, Peak Hold to GCFE Range decision		
01100	01100	Write Time Delay 2, GCFE Range decision to ADC sample		6 bits
11100	11100	Read Time Delay 2, GCFE Range decision to ADC sample		
01101	01101	Write Time Delay 3, ADC Conversion time		8 bits
11101	11101	Read Time Delay 3, ADC Conversion time		
01110	01110	Write Digital to Analog Converter (DAC) setting		16 bits
11110	11110	Read Digital to Analog Converter (DAC) setting		
01111	01111	Write GCRC configuration register	A5	2 bits
11111	11111	Read GCRC configuration register		
10000	10000	Read Status Register		4 bits
10001	10001	Read 16 bits of Last Command Error		16 bits

Table 7 defines the command function bit patterns for the AFEE. The number of effective data bits, (number of register bits) is shown in the column to the right. For writes and reads of less than 16 data bits, the data word most significant bits are packed with zeroes. The GCRC configuration and status register bits are defined in **Table 8** and **Table 9**. Two bits are used to define the parity in the configuration register to reduce probability of communication failure due to single event upset.

Table 8. GCRC Configuration Register Bit Definition

Bit	Definition
0 LSB	GCRC Parity Bit A, Default value 0.
1	GCRC Parity Bit B, Default value 0. Default Parity is Odd, at least one of Parity Bit A or B is value 0. Even Parity is both Parity Bits A and B set to 1.
2	Not used.

Table 9. GCRC Status Register Bit Definition

Bit	Definition
0 LSB	TEM Trigger Parity Error occurred
1	TEM Command Address and Function Parity Error occurred
2	TEM Data Parity error occurred
3	GCFE Read Timeout
4	Not used.

7.9 Power

Maximum power draw for the combined digital and analog 3.3V interfaces is 1.5 Watts.

Maximum power draw for the PIN photodiode bias supply is 0.001 Watts.