

 GLAST LAT PROCESS SPECIFICATION	Document # <b>LAT-DS-01127-01</b>	Date Effective 23 Dec. 2002
	Prepared by(s) N. Virmani	Supersedes None
	Subsystem/Office Calorimeter Subsystem	
Document Title <b>LAT CAL AFEE Board Procurement, Quality Assurance, and Qualification Requirements</b>		

## GLAST LAT

### Calorimeter (CAL) Analog Front End Electronics (AFEE) Board

### Procurement, Quality Assurance, and Qualification Requirements

## DOCUMENT APPROVAL

**Prepared by:**

---

Nick Virmani  
Naval Research Lab

---

Date

**Approved by:**

---

W. Neil Johnson  
Naval Research Lab

---

Date

---

Jim Ampe  
Naval Research Lab

---

Date

### CHANGE HISTORY LOG

<b>Revision</b>	<b>Effective Date</b>	<b>Description of Changes</b>	<b>DCN #</b>

## TABLE OF CONTENTS

<b>1</b>	<b>SCOPE</b> .....	<b>6</b>
<b>2</b>	<b>APPLICABLE DOCUMENTS</b> .....	<b>6</b>
2.1	GOVERNMENT/MILITARY SPECIFICATIONS AND STANDARDS .....	6
2.2	OTHER PUBLICATIONS .....	6
2.3	ORDER OF PRECEDENCE .....	6
<b>3</b>	<b>REQUIREMENTS</b> .....	<b>7</b>
3.1	GENERAL REQUIREMENTS .....	7
3.1.1	<i>CAL PWB drawing</i> .....	7
3.1.2	<i>Conflicting requirements</i> .....	7
3.2	DESIGN.....	7
3.2.1	<i>Tolerances of PWB Design</i> .....	7
3.2.2	<i>Plated Metallic Layers and Finishes</i> .....	8
3.3	CAL AFEE BOARD DESIGN REQUIREMENTS .....	8
3.3.1	<i>Grid System</i> .....	8
3.3.2	<i>Quality Conformance Test Circuitry</i> .....	9
3.3.3	<i>Datums</i> .....	9
3.3.4	<i>Viewing</i> .....	9
3.3.5	<i>Mechanical Requirements</i> .....	9
3.3.6	<i>Circuit Features</i> .....	10
3.3.7	<i>Lands</i> .....	12
3.3.8	<i>Mounting Holes</i> .....	12
3.3.9	<i>Test Points</i> .....	12
3.3.10	<i>Solder Fillets and Copper Plugs</i> .....	13
<b>4</b>	<b>FINISHES AND MARKINGS</b> .....	<b>13</b>
4.1	METALLIC COATINGS .....	13
4.1.1	<i>Electrolytic Copper</i> .....	13
4.1.2	<i>Tin-Lead Plating</i> .....	13
4.1.3	<i>Solder Coating</i> .....	13
4.2	ORGANIC COATINGS .....	13
4.2.1	<i>Solder Mask</i> .....	13
4.2.2	<i>Marking Ink</i> .....	14
<b>5</b>	<b>QUALITY ASSURANCE REQUIREMENTS</b> .....	<b>15</b>
5.1	GENERAL REQUIREMENTS.....	15
5.2	DEVIATIONS AND WAIVERS .....	15
5.3	PERFORMANCE SPECIFICATION .....	16
5.4	DOCUMENTATION REQUIREMENTS .....	16
5.5	MATERIAL REQUIREMENTS .....	16
5.5.1	<i>Solder Coating</i> .....	16
5.5.2	<i>Material Handling and Storage</i> .....	16
5.5.3	<i>Metal-clad Laminates</i> .....	16
5.5.4	<i>Bonding Material</i> .....	16
5.5.5	<i>Copper Foil</i> .....	16
5.5.6	<i>Electrodeposited Copper</i> .....	17
5.6	REGISTRATION (INTERNAL AND EXTERNAL) .....	17
5.7	OUTGASSING .....	17
5.8	LAMINATE INTEGRITY .....	17
5.9	COUPON REQUIREMENTS.....	17
5.9.1	<i>Coupon Placement</i> .....	17
5.9.2	<i>Coupon Design</i> .....	17
5.9.3	<i>Coupon Evaluation</i> .....	17

5.9.4	<i>Plating Integrity (as produced)</i>	18
5.9.5	<i>Plating Integrity (as received)</i>	18
5.9.6	<i>Plated-Through Hole Integrity after Thermal Stress</i>	18
5.9.7	<i>Plating Voids</i>	18
5.9.8	<i>Test Coupon Identification</i>	18
5.10	ETCHBACK	19
5.11	DRILLING	19
5.12	REPAIRS	19
5.13	QUALIFICATION REQUIREMENTS	19
5.14	SOURCE INSPECTION	19
5.15	QUALITY CONFORMANCE	19
5.16	QUALITY VERIFICATION INSPECTION	19
5.17	PWB MANUFACTURER CERTIFICATION	19
5.17.1	<i>General</i>	19
5.17.2	<i>Procuring activity on-site validation</i>	20
5.17.3	<i>Qualification of PWB</i>	20
5.17.4	<i>Lot date code</i>	20
5.17.5	<i>Printed Wiring Board Materials</i>	20
5.17.6	<i>Process Traceability</i>	20
5.17.7	<i>Production Lot</i>	20
5.17.8	<i>Process Control</i>	20
5.17.9	<i>Process Monitoring</i>	21
5.17.10	<i>Noncompliant PWB</i>	21
5.17.11	<i>Rework</i>	21
5.17.12	<i>Repair</i>	21
5.17.13	<i>Incoming Inspection at NRL</i>	21
5.18	INSPECTION LOT	21
5.18.1	<i>Traceability</i>	21
5.19	CONTRACT SERVICES	21
<b>6</b>	<b>PACKAGING AND SHIPPING</b>	<b>22</b>
6.1	INDIVIDUAL WRAPPING	22
6.2	SHIPPING CONTAINER	22
<b>7</b>	<b>TRAINING</b>	<b>22</b>
7.1	SUPPLIER RESPONSIBILITY	22
7.1.1	<i>Specification Training</i>	22
7.1.2	<i>Process Training</i>	22

## 1 SCOPE

This specification establishes the procurement, quality assurance, performance and qualification requirements for Analog Front End Electronics (AFEE) Printed Wiring Board (PWB) used on the Calorimeter (CAL) subsystem. Verification of PWB is accomplished through the use of product assurance provisions defined herein. Detail requirements, specific characteristics, and dimensions of the PWB, are specified in the PWB drawing.

## 2 APPLICABLE DOCUMENTS

### 2.1 Government/Military Specifications and Standards

The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the applicable issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS), and the applicable supplement thereto, in effect on the date of the procurement.

MIL-P-13949	General Specification for Plastic Sheet, Laminated, Metal Clad Printed Wiring Boards
MIL-STD-130K	Department of Defense Standard Practice Identification Marking of U.S. Military Property
MIL-STD-1686	Department of Defense Standard Practice Electrostatic Discharge Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment
QQ-S-571	Solder, Tin Alloy, Lead-tin Alloy, and Lead Alloy
NASA-RP-1161	Evaluation of Multilayer Printed Wiring Boards by Metallographic Techniques
S312-P-003	GSFC Procurement Specification for Rigid Printed Boards for Space Application and other High Reliability Uses

### 2.2 Other Publications

The following documents form a part of this specification to the extent specified herein. The applicable issues of these documents shall be that or those in effect by the responsible industry association or society on the date of the procurement documents.

AMS-P-81728	Plating, Tin-Lead (Electrodeposited)
ASME Y14.5	Dimensioning and Tolerancing
ASTM-E-595	Standard Test Methods for Total Mass Loss and Collected Volatile Condensable Materials for Outgassing in a Vacuum Environment
IPC-2221	Generic Standard on Printed Board Design
IPC-2222	Sectional Design Standard for Rigid Organic Printed Boards
IPC-A-600	Acceptability of Printed Boards
IPC-SM-840	Qualification and Performance of Permanent Solder Mask
IPC-TM-650	IPC Test Methods
IPC-6012	Qualification and Performance Specification for Rigid Printed Wiring Boards

### 2.3 Order of Precedence

In the event of a conflict between the procurement document(s), the text of this document and the references cited herein, the following order of precedence, shall apply:

- 1) Contract or purchase order.
- 2) CAL AFEE PWB drawing

- 3) This specification
- 4) Other documents referenced herein

### **3 REQUIREMENTS**

#### **3.1 General requirements**

PWB furnished to this specification shall conform to the requirements of the CAL AFEE drawing, this specification, and IPC-2221 and 2222, PWB design specifications. The detailed requirements contained in this section are determined by examining specific quality conformance test circuitry (test coupons), shall apply to all coupons and delivered PWBs. Defects or anomalies noted on coupons or sample PWBs (or both) when performing the inspections defined herein shall be recorded and the proper corrective actions shall be initiated to eliminate the defects or anomalies.

##### **3.1.1 CAL PWB drawing**

PWBs delivered under this specification shall be of the material, design, and construction specified on the CAL AFEE PWB drawing. If individual design details are not specified on the drawing, then the baseline design parameters shall be as detailed in the design standard IPC-2222.

##### **3.1.2 Conflicting requirements**

In the event of conflict between the requirements of this specification and other requirements of the drawing, the precedence in which documents shall govern, in descending order, is as follows:

- a. The drawing. Additional acquisition requirements may be provided in the order or contract. Any deletion of any of the performance requirements or performance verifications of this specification not approved by the activity will result in the PWB being deemed noncompliant with this specification.
- b. This specification.
- c. The applicable IPC design standard.
- d. Specifications, standards, and other documents referenced in section 2.

#### **3.2 Design**

PWB shall be of the design as specified on the drawing. If individual design details are not specified on the applicable drawing, then the baseline design parameters to be used for acceptability of finished product requirements shall be as detailed in IPC-2221 and 2222 that was used to design the PWB.

Test coupon design, quantity, placement, and usage shall be in accordance with IPC-2222 and this specification.

##### **3.2.1 Tolerances of PWB Design**

PWB materials are unstable to some degree, perfect multilayer alignment cannot be achieved. Designs of PWB shall accommodate these variations during manufacturing. PWB vendors are allowed to use their own internal standards for these variations. The following variations are for reference only:

- After etch shrinkage: 0.001 in/in
- Artwork variation: 0.0002 in/in from humidity and temperature effects (plotting error plus film base instability, unless the base is glass).
- Pinning: each occurrence, 0.002 in.
- Lamination: 0.003 in.
- Hole-to-hole in drilled patterns: 0.002 in.

Artwork factoring to compensate for material movement after etch is almost mandatory; thoughtful material choice at the design stage, plus clear definition of the material and quality requirements in drawing notes, is essential to close the control loop. Optional alignment to etched fiducials is one of the methods for reducing alignment errors, which reduces the effect of artwork pinning errors and after-etch shrinkage.

### 3.2.2 Plated Metallic Layers and Finishes

- 1) Copper (electrolytic)
  - Minimum purity: 99,5 %.
  - Minimum ductility: 12 % (18 % is recommended).
  - Minimum thickness of plated copper in plated-through holes: soldering holes 25  $\mu\text{m}$  and via holes 20  $\mu\text{m}$ .
  - Minimum thickness of basic and plated copper on surface layer for soldering pads: 40  $\mu\text{m}$ .
  - Minimum thickness of basic and plated copper for internal layer: 17,5  $\mu\text{m}$ .
- 2) Electroplated tin-lead thickness over copper
  - Before reflow: (15  $\pm$  7)  $\mu\text{m}$  is recommended.
  - After reflow:
    1. A minimum of 2  $\mu\text{m}$  is required on angle of hole corners (1  $\mu\text{m}$  is tolerated);
    2. A minimum of 8  $\mu\text{m}$  is required on half the height of the hole wall and a minimum of 2  $\mu\text{m}$  is required on the rest of the hole wall;
    3. A reflow over the pad and conductor edge is recommended, but not required.

## 3.3 CAL AFEE Board Design Requirements

### 3.3.1 Grid System

The grid system used shall match the requirements of the CAL AFEE Master Drawing. Any and all pattern features not controlled by hole locations shall be adequately dimensioned on the layout, either specifically by notes, or by reference to the grid system used to design the board. Similarly, when component locations do not end on grid, defining their locations is critical. Thus, their centerlines must be drawn or accurately defined on the layout.

Unless otherwise specified on the master drawing, the choice of the modular grid system used in the design of printed wiring boards shall be in accordance with the following:

- A modular grid system to identify all holes, test points, lands, and overall board dimensions with modular units of length of 0.100, 0.050, or 0.025 or other multiples of 0.005 inch in that order of precedence.
- For designs where the majority of the component locations are metric based, the basic units of modular length shall be 2.0, 1.0, 0.5, or other multiples of 0.1mm in that order of precedence.
- The grid systems shall be applied in the X and Y axis of the Cartesian coordinates.
- The grid shall not be reproduced on the master drawing; but may be indicated using grid scales or X, Y control dimensions.

Critical pattern feature, which may affect circuit performance such as distributed inductance, capacitance effect, and so forth, shall also be dimensioned.

### **3.3.2 Quality Conformance Test Circuitry**

Test coupons are required on all artwork and Master Drawings. The quality conformance test circuitry is comprised of the coupons and shall be a part of every panel used to produce printed-wiring boards that are designed to this standard. The minimum number of coupons per panel and the requirements for positioning will be in accordance with this specification. All other coupons may be positioned at the optional locations. All coupons required shall be shown on the master drawing, artwork, and production master.

### **3.3.3 Datums**

Datum features indicate the origin of a dimensional relationship between a toleranced feature and a designated feature or features on the printed board. Datum features are chosen to position the printed board in relation to a set of three mutually perpendicular planes.

Printed wiring board drawings shall be oriented with the component side layer 1 facing up. This orientation establishes the backside of the printed wiring board as the first (primary) of the three required datum planes. The other two datum planes (secondary and tertiary) shall be established using holes and/or etched features on the printed board. Edge datums shall not be allowed primarily because their use does not represent the function of the printed board. They may also pose producibility problems.

Datum features shall be specified on the master drawing by means of datum symbols per ASME Y14.5. The use of implied datums is not allowed.

Non-plated through holes used as datums shall be explicitly dimensioned and toleranced, even if they occur on grid. Two of these holes shall be used as datum features.

The soldermask pattern may be located by specifying a minimum land clearance or targets may be provided which serve the same function as fiducials for conductor patterns. A minimum land clearance serves the same purpose as a minimum annular ring requirement in that it tolerances the soldermask pattern location with respect to the conductor pattern.

### **3.3.4 Viewing**

Conductor layer shall be numbered consecutively, starting with component side as layer 1. When viewing from the primary side any legend on the bottom layer (secondary side) shall be mirror imaged.

### **3.3.5 Mechanical Requirements**

#### **3.3.5.1 Cutouts and Notches**

All special cutouts or notches must be designated such as not to interfere with other board features, including circuitry and lands. For routing compatibility, it is essential that cutout and notches be designed to allow for a minimum of an 0.06 inch (1.5) radius on internal corners.

#### **3.3.5.2 Bow and Twist**

Proper printed wiring board design, with respect to balanced circuitry distribution and component placement, is important to minimize the degree of bow and twist. The cross sectional layout (dielectric thickness, copper thickness and copper conductor density) should be kept as symmetrical as possible about the center of the board. The maximum allowable bow and twist for rigid boards shall be more than 0.5mm.

If symmetrical construction and tighter tolerances are not sufficient to bow requirements, stiffeners or other support hardware may be necessary and may be negotiated with the designer and procuring agency.

### 3.3.5.3 Board Edge

One board edge shall be located from a datum. Other edges may be dimensioned from that same datum, or from the located edge. They shall be dimensioned using a single dimension to maintain that relationship.

### 3.3.6 Circuit Features

#### 3.3.6.1 Conductor Spacing

Larger spacings shall be used whenever possible and the minimum spacing between conductors, between conductor patterns, and between conductive materials (such as conductive markings or mounting hardware) and shall be in accordance with Table 1 and defined on the CAL AFEE master drawing. Plated through holes passing through internal foil planes (ground and voltage) and thermal planes shall meet the requirement as specified herein and in Table 1.

**Note:** Fabrication Drawings shall contain a note indicating the minimum acceptable spacing between conductors on the finished PWB.

#### 3.3.6.2 Conductor Cross-Sectional Relationship

The width and thickness of conductors on the finished printed-wiring board shall be determined on the basis of the current carrying capacity required. For ease of manufacture and durability in usage, conductor width and spacing requirements shall be maximized while maintaining the minimum spacing requirements of Table 1. The minimum conductor width shown on the CAL AFEE master drawing shall be not less than 0.004 inch (0.10mm).

All CAL AFEE designs shall employ 1-ounce copper. Other copper thicknesses should be used only when conductor widths are restricted due to spacing, or when undesirable coupling occurs.

<b>Internal Conductors</b>			
<b>Voltage Between Conductors DC or AC Peak (Volts)</b>		<b>Minimum Spacing Internal</b>	
0 – 100		0.004 in. (0.10)	
101 – 300		0.008 in. (0.20)	
301 – 500		0.012 in. (0.30)	
Greater than 500		0.001 in. (0.003)	
<b>External Conductors</b>			
<b>Voltage</b>	<b>Coated Boards (any elevation)</b>	<b>Uncoated Boards (sea level – 10,000 ft)</b>	<b>Uncoated Boards (over 10,000 ft.)</b>
0 – 50	0.005 in. (0.12)	0.025 in. (0.60)	0.025 in. (0.60)
51 – 100	0.005 in. (0.12)	0.025 in. (0.60)	0.040 in. (1.5)

101 – 150	0.016 in. (0.40)	0.025 in. (0.60)	0.125 in. (3.2)
151 – 250	0.016 in. (0.40)	0.050 in. (1.2)	0.250 in. (6.4)
251 – 300	0.016 in. (0.40)	0.050 in. (1.2)	0.500 in. (12.7)
301 – 500	0.030 in. (0.80)	0.100 in. (2.5)	0.500 in. (12.7)
Greater than 500	0.00012 in/volt (0.002)	0.0002 in/volt (0.005)	0.001 in/volt (0.025)

**Table 1. Electrical Clearance Requirements**

### 3.3.6.3 Dielectric Spacing

Unless otherwise specified on the master drawing, the minimum dielectric spacing for all classes shall be 0.0035 inch (0.09). The minimum number of glass cloth layers between conductive layers shall be two.

### 3.3.6.4 Parallel Conductors

Closely spaced parallel conductors should be avoided to reduce etching and solder-bridging problems. Conductors should be positioned to take full advantage of available space, thus improving board quality and reproducibility.

When conductor width is reduced using automatic methods, the configuration of the transition area is determined by the end radius of the wider conductor.

Note: Long runs of parallel conductors should be avoided whenever possible because in PWB designs they act as high-frequency transformers that couple noise into other circuits.

A capacitance will form between two conductors that are parallel to each other causing potential cross talk.

Note: Impedance control considerations are also important when determining conductor width and thickness. CAL AFEE master drawings for boards shall contain a note indicating the minimum acceptable conductor width, thickness and material callouts for the final PWB.

### 3.3.6.5 Large Conductive Areas

Large conductive areas increase the likelihood for blistering or bowing during the soldering operation. Design of conductive areas should provide balanced construction and include the use of nonfunctional copper, if practical.

Large external conductive areas that extend beyond a 1 in. (25.4mm) diameter circle should contain etched areas that will break up the large conductive area but will retain the continuity and functionality of the conductor. If etched areas are not provided, other methods should be used to minimize blistering or bowing, especially during the infrared soldering (SMT) operation.

When a conductive area that extends beyond a 1 inch (25.4) diameter circle is used on an internal layer, that layer should be placed as near the center of the board as possible and shall contain etched areas that will break up the large conductive area but will retain the continuity and functionality of the conductor. If more than one internal layer has a large conductive area, the layers should be located in the board so as to provide balanced construction. For producibility reasons, care should be exercised in selecting areas for etch which may cause EMI or impedance problems.

### 3.3.7 Lands

Land areas are provided at each point where a part lead or other electrical connection is attached to the Printed Wiring Board. Usually each hole through which a component lead is inserted and soldered is centered in the land.

For surface mounted parts, the land is a rectangle, which is connected to the plated-through hole through a conductor line that electrically connects the land. A separate component hole shall be provided for each lead or terminal of a part or end of a jumper wire that is to be through-hole mounted.

#### 3.3.7.1 Aspect Ratio

The aspect ratio of plated through holes plays an important part in the ability of the manufacturer to provide sufficient plating within the plated through hole. PWBs with a greater aspect ratio can be used after discussing with the PWB manufacturer the reliability of the finished PWB.

#### 3.3.7.2 Etchback

Etchback will reduce the annular ring support on internal layers of the board. Therefore, this should be taken into account when specifying plated-through hole land size. However, the maximum etchback allowed on the CAL AFEE master drawing shall not be greater than the minimum designed annular ring nor exceed 0.003 inch (0.084mm) whichever is less. It is preferable to have etchback to not more than 0.0005" to avoid plating fold. All holes and internal layers shall be smear free.

#### 3.3.7.3 Nonfunctional Lands (Internal Layers)

It is preferred that nonfunctional lands are not to be used on Multilayer Printed Wiring Boards. They shall not be used where electrical clearance requirements do not permit, such as, ground planes, voltage planes and thermal planes. Plated through holes passing through internal foil planes (ground and voltage) and thermal planes shall meet the same minimum spacing requirements as that for conductors on internal layers.

### 3.3.8 Mounting Holes

Circuit board mounting holes may be reinforced by a surrounding land of copper, except where there is a possibility of electrical shorting.

Tooling holes are typically  $0.125" \pm 0.002"$  drilled holes. Edge to board spacing shall not be less than 0.050 in.

### 3.3.9 Test Points

Test points for probing shall be provided as part of the conductor pattern and shall be identified on the master drawing and the assembly drawing and shall not be covered by solder mask. These "probe points" shall require that a land be available for probing as opposed to a conductor. Vias or component lead mounting lands may be considered as probe points provided that sufficient area is available for probing and maintaining the integrity of the via or component lead mounting joint.

**Note:** Component lead mounting pads shall not be considered as probe points for surface mounted type boards.

### **3.3.10 Solder Fillets and Copper Plugs**

Solder may be prevented from entering the via holes by prefilling these holes with an appropriate polymer plug, covering the holes with a sheet of permanent bonded material or plating these holes with copper plating that will prevent solder access to the hole. All techniques must have sufficient durability so as to not break up when exposed to the solder process. The printed-wiring assembly drawing shall define the absence of such solder plug requirements.

Solder plugs are not necessarily required in any plated-through via hole covered with permanent solder mask, other polymeric cover layer (not conformal coating) or is already filled with an appropriate polymer in order to prevent hole access during SMT soldering.

## **4 Finishes and Markings**

### **4.1 *Metallic Coatings***

The primary function of all metallic coatings used in circuit board manufacturing is to allow for the passage of the electronic signal from point to point. Beyond this primary function, the metallic coatings offer such additional benefits as corrosion prevention, solderability enhancement, wear resistance and others. The circuit finish and other depositions shall be one or a combination of the following plating materials and as specified on the master drawing.

#### **4.1.1 Electrolytic Copper**

Copper plating is used for building up the copper deposits (thickness) on the surface and through the drilled holes to a required thickness. Electrodeposited copper plating shall be in accordance with IPC-2221 and 2222 and as specified herein. The purity of deposited copper, tensile strength, and percent elongation shall be in accordance with this specification. Thickness of electrodeposited copper shall be 0.001 inch (0.025mm)

#### **4.1.2 Tin-Lead Plating**

Tin-lead plating shall be in accordance with AMS-P-81728 and shall be 50 - 70% tin with the balance being lead. Tin-lead plating shall be 0.0003 inch (0.007mm) minimum as plated on the surface. Tin-lead plating shall be fused. This fusing operation results in the formation of a true alloy on the surface and in the through hole.

#### **4.1.3 Solder Coating**

Unless otherwise specified on the master drawing, solder coatings shall be in accordance with composition SN63 of QQ-S-571. The solder coating thickness shall be 0.0001 inches thick (0.0025mm) minimum. Solder coatings are the preferred final finish for solder mask over bare copper (SMOBC) boards and also for surface mounted printed wiring boards.

### **4.2 *Organic Coatings***

#### **4.2.1 Solder Mask**

Solder mask is a polymer coating which can be selectively applied on PWBs for the primary purpose of masking the board to limit the areas on which solder may be applied. Secondary uses may include any or all of the following:

- Physical protection

- A moisture barrier to prevent electromigration
- Improvement of insulation resistance a An insulator
- A thermal barrier during wave soldering

When properly cured, the material becomes a permanent part of the printed wiring board and shall meet the requirements of IPC-SM-840, Class 3 solder mask. The materials shall be type B, Dry Photo defined Image

The use of solder mask shall be specified on the CAL AFEE printed wiring board drawing. The conductor areas under the solder mask should be bare copper, oxide treated copper, or plated with other non-melting metals. All exposed conductor areas (lands, plated through-holes, etc.) must be coated with solder or fused tin-lead.

The size of the openings in the solder mask are determined by the solder mask artwork. The land size opening on the Master Drawing or artwork shall be line to line fit with the tolerance specified on the Master Drawing.

Recommended tolerances are:

Photoimageable = +0.003 (0.08), -0.000 (0.00)

Via holes shall be either covered (tented) with a permanent dry film solder mask (IPC-SM-840, type B, class 3). When tenting over vias is used, the preferred finished hole diameter of the vias shall be 0.025 inch (0.64) or .035 inch (0.90) maximum (acceptable). Tenting of the via holes shall be accomplished so that the hole is covered on both sides.

## **4.2.2 Marking Ink**

Marking inks may be used to provide identification marking on the printed board, to provide reference designator, part numbers, revision status, orientation / polarization symbols, bar codes, etc. Marking inks shall be nonconductive nonnutrient and shall be able to withstand assembly processes and shall, when required be visible at the assembly level. Legends shall be of sufficient size and clarity to optimize their usage. When conductive black ink is used, the marking shall be treated as a. conductive element on the board. Marking inks typically used on printed wiring boards can be applied over solder mask. However, compatibility of the ink with the solder mask should be verified before it is used in production.

### **4.2.2.1 Marking Locations**

The intent of a reference designation is to identify and locate the component parts. When reference designators are used, the markings should be placed where they can be seen when the components are mounted on the board. Preferred location for components with pigtail leads is immediately below the right hand lead. Markings for other parts shall be located in the least ambiguous position possible below, above, or to one side of the component. Markings should read either parallel to the bottom or to the right side of the board, according to the horizontal or vertical orientation of the component. In no case should marking be placed directly under a component or placed such that other parts will cover or obscure the visibility of the marking.

No marking produced through silkscreening, rubber stamp or stencil shall touch or be placed on conductors, ground planes or other metallic surfaces except when covered by a solder mask. Etched markings are acceptable on the board and in ground planes providing electrical integrity is not compromised.

Part number, serial number, assembly number and revision shall be placed in the most visible area on the board, preferably across the top of the card. Part number and assembly part number shall be in

accordance with MIL-STD-130K.

#### **4.2.2.2 Required Markings**

All reference designations, component outlines, board part number, assembly part number, serial number, revision letters, Pin 1 indicators, tab locators, capacitor and diode polarities, terminal numbers (unless otherwise identified), and first and last connector pin numbers should be placed on the boards provided no location violations occur. This will reduce both assembly labor and rework.

If it is not possible to place all the markings listed above on the board, the following should be placed on the board as a minimum:

- 1) Pin 1 locators
- 2) Tab locators
- 3) Capacitor and diode polarities
- 4) Terminal numbers
- 5) Reference designations for variable resistors and capacitors.
- 6) Test point numbers
- 7) First and last connector pin numbers
- 8) Commercial and Government Entity (CAGE)

Part numbers, serial numbers (if required), and revision letters shall also be marked if at all possible in lieu of bag and tag.

#### **4.2.2.3 Marking Height**

A character height of 0.100 inches (2.54) on the reduced to actual size drawing shall be used as a standard. A minimum character height of 0.06 inches (1.5) may be used where space limitations dictate. At least 0.005 inch (0.127) clearance (including non-conductive marking material) shall be maintained between the marking and any part of the etched circuit exposed from solder mask. In all cases, however, the height of reference designations shall be uniform throughout the printed circuit board.

#### **4.2.2.4 Detailed Board Marking**

Printed wiring assemblies shall be marked in accordance with MIL-STD-1686. The marking shall be etched or applied by the use of a permanent ink, which will withstand assembly processing. Additional markings if required shall be specified on the assembly drawing.

## **5 Quality Assurance Requirements**

### **5.1 General Requirements**

Printed boards furnished to this specification shall conform to the requirements of the master drawing, this specification, IPC-2221, IPC-2222, and IPC-6012. The detailed requirements contained in this section, although determined by examining specific quality conformance test circuitry (test coupons) and sample printed boards, shall apply to all coupons, sample boards, and delivered printed boards. Defects or anomalies noted on coupons or sample boards (or both) when performing the specified inspections shall be recorded and the proper corrective actions shall be initiated to eliminate the defects or anomalies.

### **5.2 Deviations and Waivers**

Deviations and waivers to the contract or purchase order, Printed Board Master Drawing or this specification shall be submitted to the procuring activity for approval. *Written approval of any deviation or*

*waiver shall be obtained prior to delivering product.*

### **5.3 Performance Specification**

All printed boards shall be procured to the design requirements of this specification, IPC-2221, IPC-2222, and IPC-6012. Procured boards shall be Classes 3 Reliability Electronic Products, per IPC-2221, IPC-2222, and IPC-6012. All PWBs procured to this specification shall meet the requirements as defined herein. If the requirements are not defined in this specification, then IPC-6012 shall be used as a guideline.

The following printed board defect(s), permitted under IPC-2221, REQUIREMENTS, are not allowed for product supplied to this specification:

- Pink Ring - Pink ring is not allowed.
- Exposed Weave - Exposed weave shall not be allowed in as-received boards.

### **5.4 Documentation Requirements**

Documentation supplied to the printed board manufacturer shall be in accordance with IPC-2222.

### **5.5 Material Requirements**

Material requirements shall be as specified in the master drawing, this specification and IPC-2221 and 2222.

#### **5.5.1 Solder Coating**

Solder coating shall be in accordance with IPC-2221 and 2222 and this specification.

#### **5.5.2 Material Handling and Storage**

Material handling and storage shall be in accordance with IPC-2221, IPC-2222, IPC-6012 and any applicable manufacturers data sheets. Raw material storage and handling shall be controlled to insure and prolong shelf life. When released from primary storage areas, material shall be handled and controlled to minimize contamination and damage.

#### **5.5.3 Metal-clad Laminates**

Unless otherwise specified, metal-clad laminates for PWBs shall be in accordance with MIL-P-13949, type GIN (polyimide). When an epoxy resin system is required, the metal-clad laminate shall be in accordance with MIL-P-13949 and have a glass transition temperature (T<sub>g</sub>) above 150°C (302°F). Other materials shall not be used without prior approval.

#### **5.5.4 Bonding Material**

The inner-layer bonding material for PWBs shall be preimpregnated (B-Stage) and of the same type as the base laminate.

#### **5.5.5 Copper Foil**

Unless otherwise specified on the CAL AFEE drawing, the copper foil shall be Class 3 high temperature elongation (HTE) in accordance with IPC-2221 and 2222. The thickness shall be as specified in the

master drawing.

### **5.5.6 Electrodeposited Copper**

The electrodeposited copper shall have an elongation as specified herein and an average tensile strength of  $25.3 \times 10^6$  kg/m<sup>2</sup> (36,000 psi) minimum when measured in accordance with IPC-TM-650 Method 2.4.18. Tensile strength and elongation shall be monitored bi-weekly and the data from the most recent evaluation shall be used to determine acceptability.

### **5.6 Registration (Internal and External)**

Registration shall be as described in IPC-2221 and IPC-6012 *except* that the minimum internal and external annular ring shall be 50 mm (0.002 in) for all plated through-holes (including vias).

### **5.7 Outgassing**

When tested in accordance with ASTM Test Method ASTM E-595, no material shall have a total mass loss (TML) greater than 1.0% and a collected volatile condensable material (CVCM) greater than 0.1%. Each material (for example, Laminate material and solder mask) shall be tested separately. Foil shall be removed from laminate material prior to test. Certified test data provided by the material manufacturer or by an approved test laboratory is acceptable.

### **5.8 Laminate Integrity**

Laminate integrity shall be as described in IPC-2221 and 2222, for products. Laminate voids or cracks exceeding 75 µm (0.003 inch) in the unstressed coupon are *not* acceptable. Laminate voids shall be defined to include resin recession.

### **5.9 Coupon Requirements**

Coupon requirements shall be as specified in IPC-2221 and 2222 *except* that a total of six (6) 'B' coupon segments per panel are required. The coupons shall not be separated from the panel prior to completing all board manufacturing processes. Using production boards in lieu of coupons shall require prior procuring activity approval. A 100% coupon evaluation is required for Types 3 boards.

#### **5.9.1 Coupon Placement**

Coupon(s) shall be placed as specified in IPC-2221 and 2222.

#### **5.9.2 Coupon Design**

Coupons shall be designed in accordance with IPC-2221 and 2222. Each layer of the printed board shall be represented by internal annular rings at all coupon plated-through holes. When thermal relief is used in the board, the same thermal relief design shall be used in the coupon.

#### **5.9.3 Coupon Evaluation**

Coupons shall be evaluated in accordance with the requirements of this specification, IPC-2221, IPC-2222, and IPC-6012. When clarification of requirements is necessary, IPC-A600 shall be used. NASA-RP-1161 may be used to provide guidance in preparing and inspecting coupons.

#### 5.9.4 Plating Integrity (as produced)

The criteria specified in IPC-2221 and 2222 shall be evaluated both before and after coupon microsection etching.

#### 5.9.5 Plating Integrity (as received)

Lifted lands shall *not* be allowed in *as received* boards.

#### 5.9.6 Plated-Through Hole Integrity after Thermal Stress

Following thermal stressing, coupons shall be microsectioned and examined before and after microsection etching. They shall meet the requirements of this specification, IPC-2221, IPC-2222, and IPC-6012, for Class 3.

#### 5.9.7 Plating Voids

Any product exceeding the criteria's of IPC-2221, IPC-2222, and IPC-6012 for Class 3 product shall be rejected.

#### 5.9.8 Test Coupon Identification

- 1) Test coupons are to be identified with the following:
  - a. FSCM of board manufacturers.
  - b. Part number and revision letter of master drawing.
  - c. Board traceability and lot number.
- 2) Dimensions are in inches.
- 3) Metric equivalents are given for general information only.
- 4) Unless otherwise specified, all conductors shall be  $.020 + .003$  inch ( $0.51 \pm .08$ ).
- 5) Unless otherwise specified, the tolerances shall meet the requirements of this specification.
- 6) Unless otherwise specified, the minimum land dimension shall be  $.070 + .005$  inch ( $1.78 \pm 0.13$ ) and may represent the land shape used on the associated board. Holes in the land areas shall be the diameter of the smallest component hole in the PWB.
- 7) Coupons for surface layers or integral layers shall be representative of the type of circuitry on the associated layer. Any layer with large copper planes shall use the appropriate plane coupon where applicable on the layer that is being represented by the coupon.
- 8) Conductor layer number 1 shall be the first layer on the component side, and all other conductor layers shall be counted consecutively downward through the laminated board to the bottom conductor layer, which is the solder side.
- 9) Spacing between coupons may be modified to accommodate tooling holes used for automatic and/or multiple mounting microsectioning equipment.
- 10) The land dimension should represent the smallest land used for a component hole in the associated board.
- 11) The holes in the lands should be the diameter of the smallest components in the PWB.
- 12) The clearance hole in the planes used for the specific layer evaluation should be design dimension minus  $2 \times .002$  inch (.05). All other clearances should be a minimum of design dimension plus  $2 \times .002$  inch (.05). (Additional allowances may be made for the etch

allowances used in the PWB).

### **5.10 Etchback**

Etchback is required. Etchback shall meet the limits of IPC-2221 and 2222 and as specified herein.

### **5.11 Drilling**

The smallest-sized drill used for a plated through hole shall be used for the coupons. These holes shall be microsectioned and examined in accordance with this specification, IPC-2221 IPC-2222, and IPC-6012. The manufacturer shall have a drill replacement program in use.

### **5.12 Repairs**

Bare board repairs shall not be permitted.

### **5.13 Qualification Requirements**

Qualification testing shall be performed in accordance with the requirements of IPC-2221 and 2222.

### **5.14 Source Inspection**

NRL reserves the right to verify that all the requirements of this specification have been met. Periodic surveillance and/or inspection of all phases of fabrication, testing, and inspection may be conducted.

### **5.15 Quality Conformance**

Quality conformance inspection shall be performed by the board manufacturer in accordance with the requirements of IPC-2221. PWBs shall be subjected to a 100% coupon inspection and a 100% visual inspection to this specification, for all boards. Panel and boards not meeting the requirements of this specification shall be rejected.

### **5.16 Quality Verification Inspection**

Coupons from each panel shall be evaluated for structural integrity before and after thermal stress in accordance with the requirements of IPC-2221 and this specification. Coupons shall also be prepared and evaluated by GSFC and in a facility approved by GSFC.

### **5.17 PWB Manufacturer Certification**

#### **5.17.1 General**

The manufacturer of PWBs for compliance with this specification shall use production and verification facilities, and a Qualification program to assure successful compliance with the provisions of this specification and the associated specification. Adequacy of a PWB manufacturer to meet the requirements of this specification shall be determined by the NRL and procuring activity. Only PWBs that meet all the requirements of this specification, the associated specification and of the PWB procurement documentation shall be delivered.

### **5.17.2 Procuring activity on-site validation**

The validation process will involve a NRL and procuring activity review of the manufacturer's plan and self-validation results. The manufacturer shall demonstrate to the NRL and procuring activity that the Manufacturing program is being implemented to meet the requirement of this specification. Each portion of the manufacturer's process flow, including contract service operations, may be reviewed. The NRL procuring activity reserves the right to perform on-site validation surveys of facilities/technologies that the manufacturer plans to use.

### **5.17.3 Qualification of PWB**

The manufacturer shall ensure that all requirements of the associated specification, the PWB procurement documentation, PWB master drawing, and this specification have been satisfactorily met. In the event that a lot fails to pass inspection and is not dispositioned as scrap, the manufacturer shall remove the lot and store them separately from the flight lot until a resolution is reached.

### **5.17.4 Lot date code**

Unless otherwise specified, the PWBs shall be marked by a unique code to identify the period during which PWBs in that production lot were manufactured. The marking method used and time of application of the lot date code shall be as defined herein. The first two numbers in the code shall be the last two digits of the number of the year, and third and fourth numbers shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or from top to bottom, the code number shall designate the year and week, in that order (e.g., 9714 equals week 14 of 1997).

### **5.17.5 Printed Wiring Board Materials**

Traceability shall be such that for each production lot of PWBs, all PWB materials specified or used shall be traceable to a material production lot, inspection lot, or other specified grouping.

### **5.17.6 Process Traceability**

Each PWB, or each group of PWBs that has been fabricated as a production lot, shall be identifiable such that the complete manufacturing history shall be traceable. The history should include, as a minimum, the performance date of all identified production process steps, the procedure specification, any rework steps, and the identification of the equipment used and operator performing the process steps.

### **5.17.7 Production Lot**

The manufacturer shall maintain production lot traceability for all PWBs. Each test coupon shall be identifiable with those corresponding PWBs produced on the same panel. All separated individual test coupons shall have their traceability maintained back to the production panel or qualification test vehicle from which the test coupons were separated.

### **5.17.8 Process Control**

The manufacturer shall establish and maintain process production controls, quality controls and inspections at appropriately located points in the manufacturing process to assure continuous control of quality of materials, individual layers and assembled layers including contract service operations and testing. These controls and inspections shall be adequate to assure compliance with the PWB procurement documentation and quality requirements of PWBs manufactured to this specification and the associated specification.

### **5.17.9 Process Monitoring**

A process monitoring system shall be used by the manufacturer to control key processing steps to insure product yield and process reliability. The monitoring system can use various test vehicles, methods and measurement techniques. The critical operations to be monitored shall be determined by the manufacturer based on its experience and knowledge of its processes. The resulting data shall be analyzed by appropriate process control methods to determine control effectiveness.

#### **5.17.10 Noncompliant PWB**

PWBs produced to acquisition documents that take exception to any of the requirements, inspections, and tests specified herein and in the associated specification that are not specifically detailed and approved by the NRL and procuring agency. Noncompliant PWBs shall not be shipped.

#### **5.17.11 Rework**

The act of repeating one or more manufacturing operations, or performing alternative techniques in order to bring a product into compliance with applicable drawings and specifications shall not be performed without prior approval from the NRL and procuring activity.

#### **5.17.12 Repair**

The act of restoring the functional characteristics of a defective product without restoring the compliance with applicable drawing or specifications shall not be performed.

#### **5.17.13 Incoming Inspection at NRL**

Procedures should be in place at NRL to insure conformance of the PWB material to the applicable PWB material acquisition documents or material specifications. Inspection reports, certificates of compliance and test data should be maintained on file for review by the qualifying activity.

### **5.18 Inspection Lot**

An inspection lot shall consist of all printed boards having the same part number, fabricated from the same materials, using the same processes, produced under the same conditions, accompanied by the same routing documentation and submitted for quality conformance inspection at the same time.

#### **5.18.1 Traceability**

The manufacturers shall establish and maintain a traceability program for all printed boards in accordance with IPC-2222. Each separated coupon shall be traceable to the panel from which it was separated. Each board shall be identified with a unique serial number and be traceable to its panel.

### **5.19 Contract Services**

If the manufacturer contracts any portion of his manufacturing operation to a contract service, he shall notify NRL in writing prior to fabricating any boards. The manufacturer shall flow down the requirements of this specification to any contract service.

## **6 PACKAGING AND SHIPPING**

### **6.1 Individual Wrapping**

Each printed board shall be wrapped in a suitable material and secured in groups to prevent abrasion damage during transport. The wrapping material shall be constructed from material that will not contribute to degraded solderability of the printed board for a three year storage period under ambient conditions.

### **6.2 Shipping Container**

The boards shall be protected adequately during shipment by using suitable packing materials and placing them in a shipping container or box to support the boards during transport.

## **7 Training**

### **7.1 Supplier Responsibility**

The supplier shall be responsible for the following:

#### **7.1.1 Specification Training**

All printed board manufacturing and inspection personnel who work on product procured to this specification shall be familiar with this specification, IPC-2221 and 2222 and other pertinent requirements of the engineering and procurement documents.

#### **7.1.2 Process Training**

Training shall be provided to manufacturing and inspection personnel in the techniques of printed board fabrication and inspection to assure each individual is appropriately skilled in the processes for which they are responsible in their assigned work.