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*** WBS 4.1.5 CALORIMETER (N. Johnson/Carosso)

4.1.5.1 CAL Management

Completed PMCS loading, detail updates continuing
Discussion of EM scope is continuing
Reviewed French documentation for CNES PRR

France
Preparing CNES PRR scheduled for November 6th

4.1.5.3 Mission Assurance

- Working on bonding issue related to voids and integrity of bond after French method of cutting bonds.
- Had meeting with GSFC materials engineer to discuss the bonding specification and to discuss test methods.
- Working with GSFC/SLAC and other design engineers to resolve parts issues. It was a very productive week with respect to locating qualified parts to avoid additional cost of testing.
- First draft of material lists, inorganic and polymeric for CAL and tracker were emailed to SLAC. This list will be constantly updated.
- First draft of EEE parts list for CAL, ACD, and TKR will be emailed to SLAC during next week and will be updated before Thanksgiving prior to formal submission to GSFC through SLAC.
- CAL FMEA work is progressing well and hope to complete the report prior to Thanksgiving.
- Visual inspection of crystal and PIN photodiode bonding was performed at NRL and will be photographed next week.
- Soldering of flex to CAL EEE board and alternative method of attachment are being tried and samples will be presented during next week meeting at NRL.
- Locating suppliers for assembly of CAL EEE board.

4.1.5.4.5 Simulations

Continued discussion of particle rates in LEO. We should compare CREME and CHIME inputs, intermediate results, and outputs once and for all. (NRL)

We're preparing agenda items and assigning presentations for Nov ground software meeting. Major topics will be status and future for evt reconstruction, needs and requirements for calibration s/w, and production processing. (NRL)

4.1.5.5 Crystal Detector Elements

Continued PIN bonding tests, thermal cycling of optical adhesives. Failed samples and whole bonds will be photographed to document our ability or inability to determine the bond quality by visual inspection. (NRL)

4.1.5.7 Analog Front End Electronics

Continued development of Test procedures
Continued work on digital ASIC design and test GSE

4. 1. 5. 9 Calorimeter Module Assembly, Test & Calibration

Updating calibration requirements document with do Couto e Silva. Modified and extended list of CAL calibration needs. (NRL)

4. 1. E. 3 CAL Balloon Flight

Continuing work on energy calibration algorithms. Improved calibrations will be committed start of next week. (NRL)

Continuing analysis of stability of light tapering in the 80 CsI crystals after 18 months of storage, mechanical vibration and shock, temperature cycling, humidity variation, etc etc.

A detailed checkout of the BFEM CAL will have to wait a few weeks until we can slip it into the schedule. We haven't yet successfully powered it up. (NRL)

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*** WBS 4. 1. 6 ANTICOINCIDENCE DETECTOR (Thompson/Larsen)

ACD efforts this week have concentrated in two areas:

1. Continued review of the schedule and resources. We have delivered an updated, resource-loaded schedule on Friday, November 2, and we did this despite the absence of our resource analyst. The mechanical, electrical, and test engineers who lead these areas for the ACD have re-examined all aspects of the work.
2. Planning for integration and test. In this area, we are developing our test plans and test plan matrix, we have identified many of the interfaces to other subsystems, and we are actively looking at how we would handle contingency issues such as replacing parts during integration and test. This last issue affects our spares philosophy.

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*** WBS 4. 1. 7 ELECTRONICS (Haller)

Meeting with Spectrum Astro regarding their final report for the spacecraft studies.

Still working on the controller ASIC for the tracker with single-port memory included. The memory was designed at SLAC and is being simulated and laid-out. It will be integrated into the placed&routed controller layout.

More tests at SLAC on the GCFE cal front-end chip, trying to measure performance before small run submission mid November.

Simulator (simulating front-end electronics) for the dataflow testbed was discussed and James Wallace is writing the planned solution up.

More interfacing to sub-systems regarding the inter-system links.

Working on documentation for the PDR.

Discussion (NRL/SLAC/Siver Engineering) about pros/cons of (re)starting own CPU (603E) design

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